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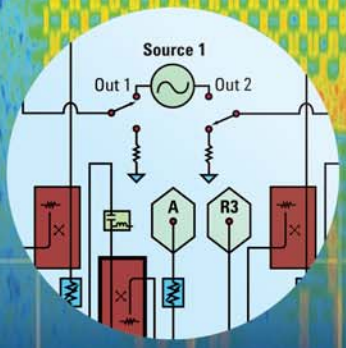
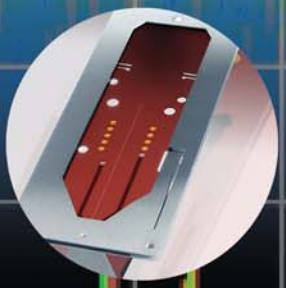
Agilent Measurement Journal





Agilent Technologies

Answering Scarcity with Abundant Innovation

Darlene J.S. Solomon
Chief Technology Officer, Agilent Technologies
Vice President, Agilent Laboratories

In many cases, it's scarcity — not necessity — that drives innovation. As our customers deal with various forms of scarcity, it spurs us to create new innovations in measurement technology.

Wireless communications is just one example. With the widespread use of cellular devices, wireless Internet access and more, it's easy to forget one essential fact: frequency spectrum is a scarce resource. The airwaves are crowded with myriad signals, many of which operate on adjacent frequencies. As new wireless applications demand additional system capacity, the radio spectrum becomes ever more crowded with the rising amounts of data carried. The result is increased interference.

Creating higher system capacity requires devising more complex protocols. But this increased complexity uses more computation, increases the power demands and reduces the battery life of wireless devices.

Further developments in managing interference are critical to increasing system capacity. Research and innovation opportunities also exist in the areas of power management, parallel computation and higher order multiple-input/multiple-output (MIMO).

Innovations in modulation, such as orthogonal frequency-division multiplexing (OFDM), continue to expand the volume of information that can be delivered through a narrow communication channel.

Agilent's ongoing improvements to our instruments using increasingly precise mixers and faster digitizers enable analysis of ever more complex modulation methods. Innovations such as vector signal analyzers (VSAs) enhance this analysis by extracting information from acquired signals according to the relevant wireless standard.

Sometimes scarcity takes on physical dimensions. In fields ranging from forensics to proteomics, successful analysis depends on the ability to work with very small or very limited samples. Rather than cubic centimeters or milliliters, the quantities are described in nanoliters and picoliters — billionths and trillionths of a liter.

Innovations that enable new measurements often occur when proven technologies from different fields are brought together. A liquid chromatograph (LC) uses an elaborate network of tubes, valves and analytical columns to separate and measure mixtures of sample substances. Semiconductor fabrication technology makes it possible to create highly precise physical structures at microscopic scales.

Agilent applied these capabilities to develop a new kind of device — the HPLC-Chip/MS — that revolutionizes the amount of information that can be obtained from even the scarcest samples. Smaller than a credit card, the HPLC-Chip/MS combines high performance liquid chromatography and mass spectrometry, which determines the composition of a molecule. With this chip, scientists can identify proteins within minutes to a few hours and easily reproduce their results. The chip also has potential uses with tiny samples in drug development, food safety and environmental monitoring.

From communications to chemistry, we see no shortage of challenges for all who seek to measure their world. However, as you'll see in this issue of *Agilent Measurement Journal*, there is no scarcity of new measurement ideas coming from the people of Agilent.

Agilent Measurement Journal

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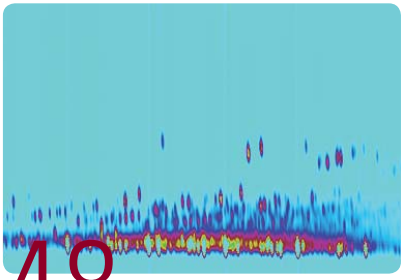

Upcoming Conferences and Events

June 2007

June 3-8, 2007
IEEE MTT-S International Microwave Symposium
Honolulu, HI
www.ims2007.org

June 4-8, 2007
44th ACM/IEEE Design Automation Conference (DAC)
San Diego, CA
www.dac.com

June 6, 2007
International Conference on Nanoscience
Beijing, China
www.chinanano.org

June 12-15, 2007
Wireless Communications Association 2007
Washington, D.C.
www.wcai.com

June 19-21, 2007
LXI Consortium General Meeting
Beijing, China
www.lxistandard.org/about/events

June 19-21, 2007
EuroNanoForum 2007
Düsseldorf, Germany
www.euronanoforum2007.de

July 2007

July 17-18, 2007
Wireless & Mobile Expo and Conference
Toronto, Canada
wirelessandmobile.wowgao.com

July 17-19, 2007
MemCon 07
Santa Clara, CA
www.memcon.com

Agilent Measurement Journal

Emerging Innovations

Nanotech visualization in education

Nanotechnology promises to transform research, product development and manufacturing in a variety of industries, and Agilent will be there to see new nanotech developments through ... literally. Our new atomic force microscope (AFM), which enables researchers to view materials at the nanoscale level, includes an Agilent-developed microscope curriculum designed to help educators introduce their students to a wide range of AFM techniques.

The cost-effective and easy-to-use Agilent 5400 AFM/SPM is a modular system providing atomic-scale resolution with high-precision control, making it ideal for various applications from materials science to nanolithography. "It proved to be a serious scientific instrument with outstanding resolution, yet has an intuitive and user-friendly software interface," says Jayne C. Garno, assistant professor of chemistry at Louisiana State University in Baton Rouge, which served as the beta test site.

The system can also be easily upgraded to the premier Agilent 5500 AFM/SPM when greater functionality is required.

Taking WiMAX analysis to the next level

WiMAX solution developers looking to outpace their competitors by launching products more quickly will benefit from the Agilent E6651 Mobile WiMAX test set. Developed with Innowireless Co. Ltd., the IEEE 802.16e integrated subscriber product test set incorporates a wide array of RF measurements for equipment characterization, collaboration and verification and allows engineers to test, stress and debug IP data handling capabilities in a laboratory environment.

Using a wider range of network parameters, the test set provides WiMAX equipment developers with a high-speed, easy-to-use Windows® XP platform. The E6651A also complements Agilent's WiMAX solutions for signal analyzers, signal generators and EDA software.

Raising the bar in DMM speed, accuracy

Test system integrators now have a 1U digital multimeter providing speed and throughput of 50,000 readings per second at 4½-digit accuracy using new A/D-converter technology. The Agilent L4411A 6½-digit high-performance DMM offers a choice of computer interfaces, including LXI. The display features "latest reading" and LAN address, allowing system integrators to integrate and debug the test system easily. Transactional input/output is up to three times faster than other modular DMMs, and triggering is both quick and precise with trigger latency and jitter less than 1 µs.

CG injects efficiency into capillary flow testing

Agilent has achieved a milestone in capillary flow technology with the Agilent 7890A gas chromatograph (GC) platform. Chemists are now able to connect, switch, split and divert capillary gas flows inside the GC oven while keeping the hardware leak-free, despite oven-temperature cycling. This application of in-oven flow technology promises to reveal a host of useful applications and productivity improvements. For instance, chemists can use up to three detectors simultaneously to better detect target substances in very complex mixtures. And because they can rely on existing chromatographic run methods, they will avoid extensive and time-consuming method development and revalidation.

The 7890A features a fifth-generation electronic pneumatics control (EPC) and digital electronics with pressure regulation to 0.001 psi. Its small mass enables the device to track oven temperature, while its unique design features low dead volume. The component's rugged connectors benefit from a new ferrule design that minimizes tailing, and channels and connectors feature highly inert flowpaths.

The 7890A is also highlighted in a May 2, 2007, entry in the Agilent *Nano Measure* blog. To view the blog and join the discussion, please visit nano.tm.agilent.com/blog/.

Turning the "triple play"

The rapid emergence of Internet protocol television (IPTV) means the wait for is over for those who can't get enough baseball — or any other programming — from the TV in their living room. Capitalizing on the right combination of market demand and innovation, network equipment manufacturers (NEMs) and service providers are rapidly implementing the triple play combination of voice, data and video services.

IPTV delivers digital programming content over broadband networks to computers and other devices — including set-top-boxes — rather than through traditional TV sets. Agilent is addressing this emerging market with the J6900A analyzer, a development, installation, maintenance and troubleshooting tool that provides essential measurements and key performance indicators. The J6900A enables engineers and technicians to identify and solve network issues such as interoperability, voice and data media transport, service delivery, quality of experience (QoE) and IP network performance all with a single device, affording a threefold increase in service efficiency.

Multipurpose RFID analysis software

The Agilent 89600 vector signal analysis software now includes RFID modulation analysis capability. In addition to analyzing popular EPCglobal Class-1 Generation-2 (EPC Gen 2) UHF signals, the Agilent 89601A software also works with other RFID signals using built-in presets or by manually setting the demodulation format, line coding and bit rate. The software provides additional flexibility by allowing measurements to be made anywhere from the baseband to the antenna on both digitized and analog signals. This creates time and cost savings by enabling system designers to use one measurement console with consistent readings, as opposed to conventional systems that require users to create different displays and measurement algorithms for each measurement.

Ensuring voice quality in 3G networks

Next-generation wireless networks boasting data speeds of 100 Mb/s will offer consumers a wealth of mobile communications and content options such as video calls and TV programming. While these advances will provide additional revenue sources for carriers, voice remains the "killer app" and call quality is their number one priority. Carriers face the delicate responsibility of ensuring today's quality levels while deploying the mix of technologies, standards and functions that comprise advanced next-generation services.

Agilent is helping carriers navigate this third-generation long-term evolution (3G LTE) with our Advanced Design System (ADS) measurement solutions. ADS provides power simulation tools that enable testing of 3G data rates without the devices being available on the network, ensuring they will work effectively when LTE is rolled out.

Labs pinpoints key breast milk component

Scientists from Agilent Laboratories and the University of California at Davis (UCD) developed a new technique for rapidly analyzing the composition of oligosaccharides (OGs), the third-largest component in breast milk. Measuring and determining the role of OGs in breast milk has been all but impossible in individual samples, due to OGs' diversity and the limitations of available research tools.

Sharing their results in an article published in the online version of the *Journal of Agricultural and Food Chemistry*, the multi-disciplinary team of engineers and scientists from Agilent Labs and UCD detailed their use of Agilent analytical tools to identify OGs in samples from five women. Agilent's glycan chip enabled scientists to perform high-resolution separation of complex mixtures, while the company's time-of-flight mass spectrometer (TOF MS) helped characterize each OG variation by accurately determining its mass at the molecular level.

Understanding the Use of OFDM in IEEE 802.16 (WiMAX)

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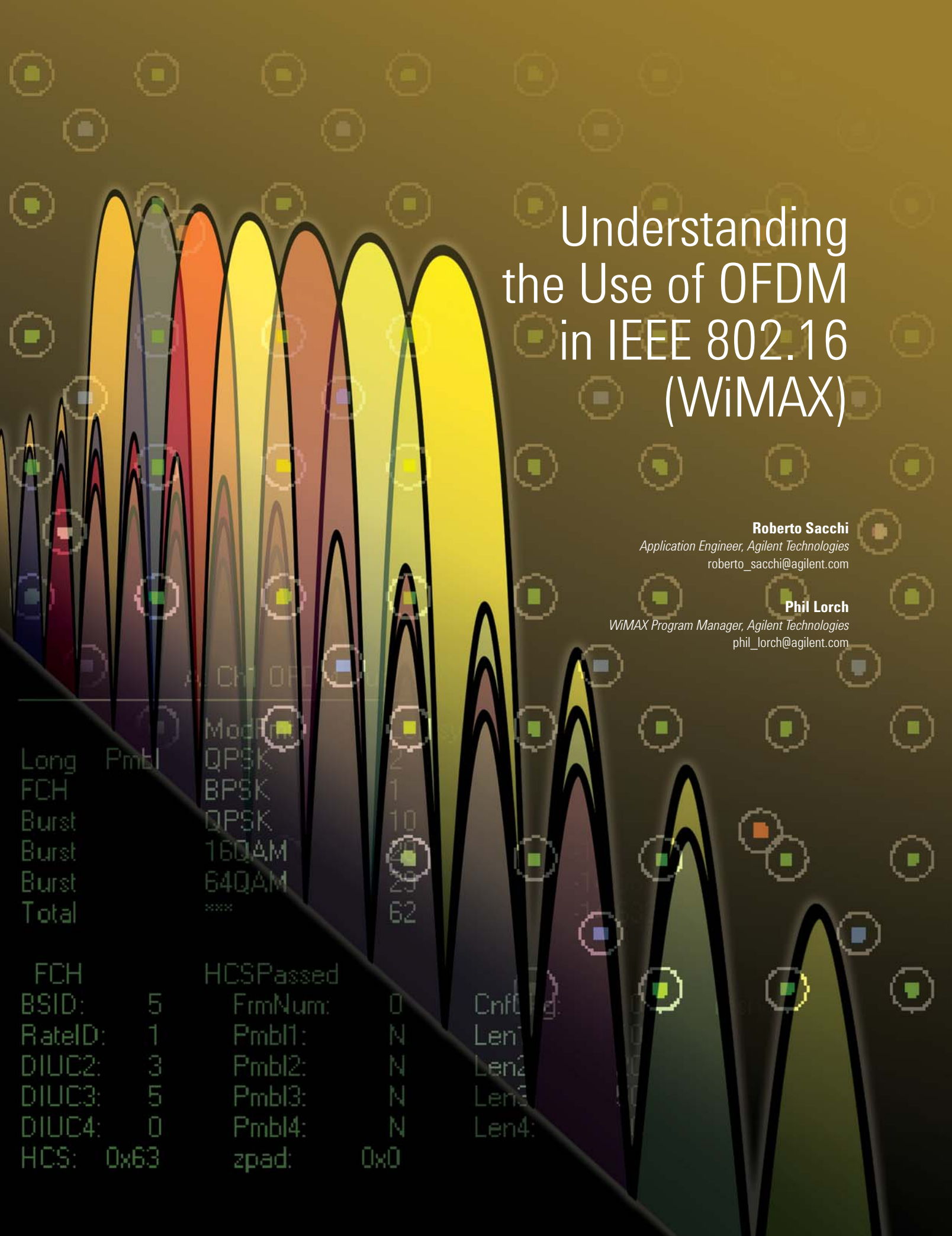

Our ability to wirelessly access the Internet from airports, shops, restaurants and hotels — or even watch TV on our mobile phones — comes courtesy of not only past advancements in radio access technology and mathematics but also present-day technology. With today's highly integrated and miniaturized radio frequency integrated circuits (RF ICs) and powerful digital signal processors (DSPs) these advancements can be economically realized.

One new broadband wireless technology gaining in popularity is IEEE 802.16 Worldwide Interoperability for Microwave Access, or simply WiMAX. Building on some of the ideas used in IEEE 802.11 wireless LAN (WLAN or Wi-Fi), WiMAX is an IP-based broadband wireless-access technology. As with Wi-Fi, WiMAX uses orthogonal frequency-division multiplexing (OFDM) and its main value is the promise of a globally standardized, spectrally-efficient and potentially lower-cost way for telecom carriers to provide fixed broadband (high speed) Internet access and other IP-based services in areas that lack wired cable or copper line telephone networks. However, it also offers much greater range than traditional 802.11-based wireless networks for reasons primarily related to how it implements OFDM.

This article provides a brief overview of how OFDM works and how it is applied in current fixed WiMAX radio designs.

Reviewing some history

In the 1930s, Bell Laboratories developed a new technique for radio-channel access that significantly enhanced the frequency-division multiplexing (FDM) schemes in use at the time. Initially known as multiple frequency-shift keying (MFSK), interest in this new method grew because it enabled efficient use of already precious radio spectrum to transmit information. Seminal technical papers on the topic were published in the late 1950s and early 1960s.[1, 2]

In one early advancement, Collins Radio developed the Kineplex Data Communication System, which achieved data transmission rates of up to 2400 bps for binary data using four equally spaced tones, each carrying data from two input channels at 300 bps.[3] References to OFDM originally appeared in a 1966 paper by Robert Chang of Bell Labs under contract to Western Electric.[4]

Today, OFDM is widely used to transmit digital data in well-established and emerging communication technologies: from ADSL over copper wire and coaxial cable for broadband Internet and video services to wireless applications such as Wi-Fi, high-definition digital radio (HD Radio) and digital video broadcasting (DVB). It is also used for ultra-wideband (UWB) applications such as WiMEDIA and Wireless USB. OFDM and its multiple access derivative, OFDMA, are now the underlying physical transport mechanism of emerging and proposed wireless communications formats such as WiMAX, Qualcomm's Ultra-Mobile-Broadband (UMB) and 3GPP long-term evolution (LTE).

Examining the basics of OFDM

OFDM relies on the principle that information can be transmitted on a radio channel through variations of a carrier signal's frequency, phase or magnitude. Rather than placing all of the transmitted information onto a single RF carrier signal, OFDM breaks down that information into smaller pieces and assigns each one to a specific *subcarrier*. Spreading the information over a large number of subcarriers makes transmissions less sensitive to typical impairments in the radio propagation environment. This approach makes OFDM an attractive method for wireless transmission of high data rate digital signals.

The fundamental principle underlying OFDM is the division of the data rate R (expressed in bps) among N parallel data subcarriers, each with a lower data rate of R/N bps. The subcarriers are offset in frequency (Δf) and are organized to prevent mutual interference using the principle of *orthogonality.*

To better understand OFDM orthogonality, it is useful to look at the basics of simple FDM for analog signals. In a typical FDM transmission, the carriers are separated somewhat in frequency by placing *guard bands* between each carrier to enable filtering at the transmitter and receiver and thus achieve reliable information recovery via classical AM/FM or PM demodulators (Figure 1).

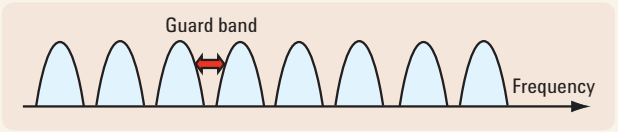

Figure 1. FDM-modulated signals in the frequency domain

OFDM spaces the subcarriers closely together without any guard bands, relying on the principle of Fourier transformation to convert digital signals from the time domain into a spectrum of frequency-domain signals that are *mathematically orthogonal* to each other. In vector terms, the dot product of two adjacent subcarriers is zero.

In radio wave propagation, orthogonal signals can be completely separated by the radio receiver, which can reject other signals in favor of the signal of interest. The frequency domain null of one subcarrier corresponds to the maximum value of the adjacent subcarrier as shown in Figure 2. This allows the subcarriers to partially overlap without interfering with each other.

Orthogonality is achieved by processing (modulating) the input digital bitstream into a complex modulated spectrum of equally spaced but orthogonal subcarriers and then converting it into a waveform that can be easily transmitted using an inverse Fourier transformation. This is one of the major benefits of OFDM: the subcarriers can be spaced very closely and actually overlap in frequency, conserving overall bandwidth (Figure 3). This is in contrast to modulation techniques such as the minimum-shift keying (MSK) method used in GSM mobile telephone services. GSM channels overlap but are not orthogonal so will interfere with each other to some extent.

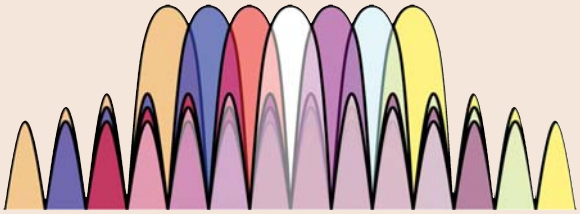

Figure 2. OFDM signal spectrum

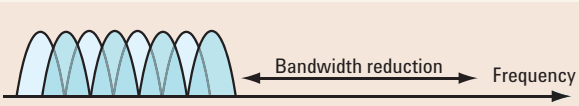

Figure 3. An OFDM signal in the frequency domain

Converting digital bitstreams into OFDM signals

To illustrate the creation of an OFDM signal, imagine that a bitstream must be transmitted through a quadrature amplitude modulation (QAM) scheme in which each symbol represents two bits. Figure 4 depicts an example set of complex symbols in the IQ plane (constellation graph): The amplitude and phase of the subcarrier are extracted from the symbol itself. In this simple case the complex value is expressed as 1 + j1.

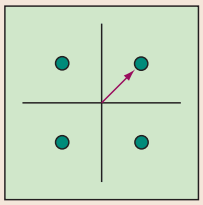

Figure 4. A symbol to be transmitted and its modulation format

In general, the N symbols to be transmitted (s_0, s_1 ..... s_{N-1}) generate N complex numbers (z_0, z_1 ..... z_{N-1}). An inverse fast Fourier transform (IFFT) is performed on this sequence of complex-valued numbers, generating a series of spectra that is then transmitted through the channel (Figure 5). This process is repeated over time, resulting in symbol *streaming* by the same single subcarrier (the specific symbol/subcarrier association is typically specified by the communications protocol). To create a multicarrier OFDM signal as in WiMAX, we extend the IFFT approach to a larger number of carriers (Figure 6).

At the receiver, the reverse process occurs. The signal is demodulated using an FFT process to convert the input — a time-varying complex waveform — back into its spectral components, recovering the initial subcarriers with their modulation and thus the original digital bitstream.

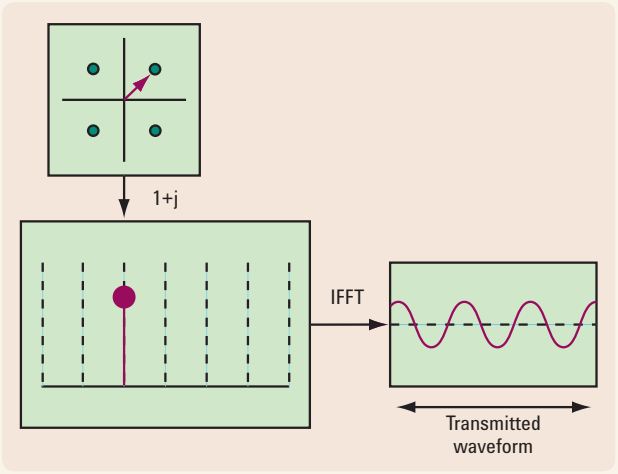

Figure 5. Construction of a single-carrier OFDM signal

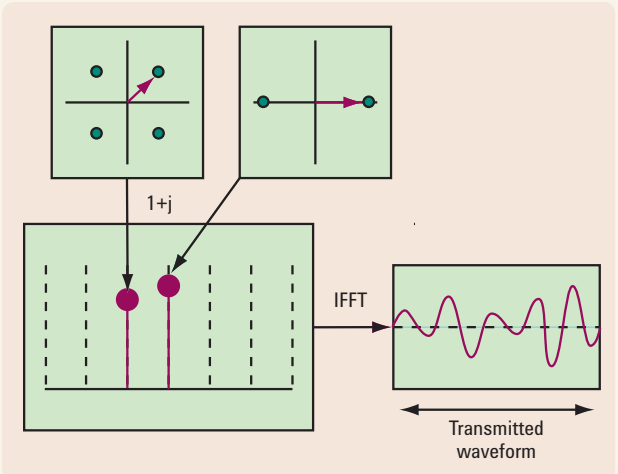

Figure 6. Generation of a multicarrier OFDM signal

Reducing symbol errors in OFDM

In addition to its high spectral efficiency, OFDM can also reduce the incidence of bit errors caused by intersymbol interference (ISI). ISI is associated with the spreading in time of digital data due to multipath effects, also known as *delay spread*. In multipath, copies of the signal arrive at different times due to reflections caused by objects in the radio propagation environment (e.g., buildings, trees, bodies of water). These delayed signals adversely affect the receiver's ability to correctly demodulate and decode the data. The higher the data rate, the shorter the time period in which each symbol can be transmitted before encountering a multipath reflection of itself.

To transmit a high data rate on a signal carrier (e.g., at broadband speeds >1 Mb/s), the length of time in which a symbol can be received and correctly demodulated is very short. To circumvent this, a guard interval (time gap) is inserted at the end of each symbol and a copy of the preceding symbol is transmitted during this time.[5]

In the case of a 10 Mb/s data rate using a single carrier, the symbol period is 1/10 MHz or 100 ns (assuming one bit is transmitted per symbol); reflections that arrive within a fraction of 100 ns will likely cause problems. However, if that same 10 Mb/s is spread over 100 OFDM subcarriers, the symbol period is now 100 x 100 ns or 10 µs and reflections that arrive within 100 ns are not a major factor. What's more, reflections that arrive within 10 µs are generally highly attenuated because they have traveled a much longer RF path (~10,000 feet). Thus, the allowable delay spread is inversely proportional to the data rate: the lower the data rate for each subcarrier, the longer the allowable delay spread. Additionally, the required guard interval in this example must be only a few hundred nanoseconds, which consumes a much smaller proportion of the signal's overall available transmission time (100 ns out of 10 µs).

Implementing OFDM in WiMAX

Figure 7. Example instruments used for WiMAX signal generation and analysis

Now let's examine the implementation of OFDM in WiMAX. To analyze the physical characteristics of the OFDM signal, it is useful to consider a WiMAX signal originating from a laboratory-grade vector signal generator (VSG) such as the Agilent MXG signal generator and evaluate it using a vector signal analyzer (VSA) such as the Agilent MXA signal analyzer running the Agilent 89601A VSA software (Figure 7).

In the IEEE 802.16-2004 standard, WiMAX is specified to operate in the 2 to 11 GHz and > 60 GHz ranges; the total occupied bandwidth can be between 1.25 and 28 MHz depending on the particular profile chosen. Profiles are used by the WiMAX Forum to constrain the range of possible devices available from different manufacturers and thereby ensure that a sufficient number of interoperable products exist for wireless operators to choose from, depending on available spectrum and local regulations. Figure 8 shows the frequency spectrum of a WiMAX signal with 7 MHz bandwidth. Note that the apparent spectral spreading of this signal is the cumulative sidelobe energy of the OFDM carriers and not spectral regrowth or adjacent channel power (ACP) due to distortion.

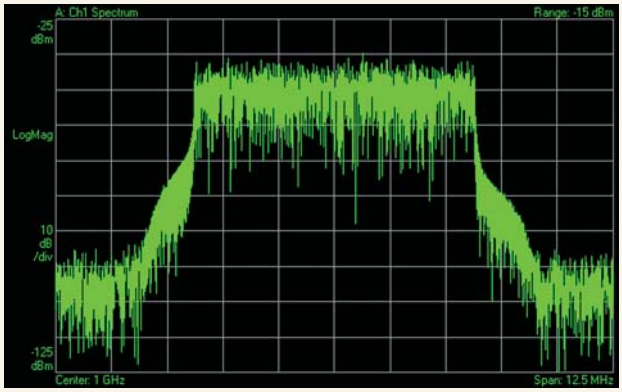

Figure 8. Frequency spectrum of a WiMAX signal with 7 MHz bandwidth

The WiMAX standard provides for a variable number of subcarriers of three types: pilot, data and null (unused). In the 256-carrier case, 56 unused carriers function as guard carriers and the other 200 are fully utilized: 192 to transport data and eight for pilots.

The pilot carriers always use binary phase-shift keying (BPSK) modulation for maximum robustness. The location and content of these carriers is known to the receiver so they can be used as a continuous reference for demodulating the data carriers.

For the data subcarriers, the standard specifies the use of four different modulation methods, depending on channel conditions: BPSK, quadrature phase-shift keying (QPSK), 16QAM and 64QAM (using different amplitudes, the QAM constellations do not overlap). The modulation scheme associated with the data subcarriers can change dynamically depending on the state of the channel. During the start of each transmission, the channel is evaluated and, to the extent possible, the next-higher-order modulation is implemented until channel throughput is maximized under the current conditions. This *adaptive modulation* capability has two key benefits:

- The transmitter can maximize the data rate for highest transmission speed for a given range in locations where there is good signal-to-noise ratio and few radio propagation issues, for example when there is good visibility between the transmitter and receiver (e.g., LOS conditions).

- The transmitter can sacrifice data rate in favor of robust transmission with low error rates for a given range when there are channel disturbances such as fading (typically non-line of sight or NLOS).

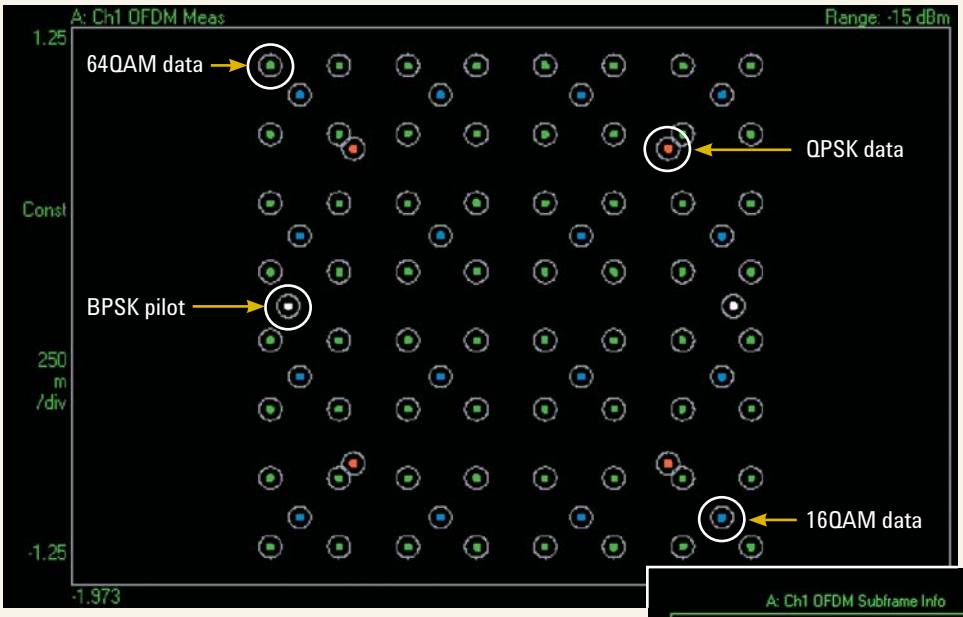

Figure 9. Composite WiMAX constellation including BPSK, QPSK, 16QAM and 64QAM

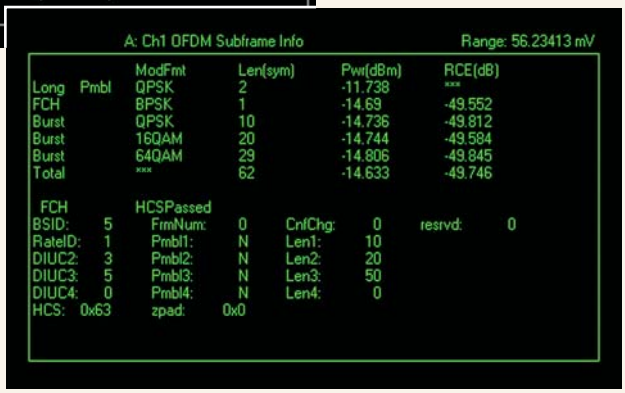

Figure 10. Subframe summary from VSA-based analysis of a WiMAX frame

Figure 9 shows a constellation analysis of a WiMAX signal containing all the modulation types specified by the standard. Modulation analysis performed with a VSA (Figure 10) reveals all modulation types present in that particular portion of the frame.

Examining the fixed WiMAX frame structure

The IEEE 802.16-2004 standard specifies two duplexing modes for downlink and uplink: time-division duplex (TDD) and frequency-division duplex (FDD). With TDD, the downlink burst is followed by one or more uplink bursts, resulting in a frame with a total duration of 2.5 to 20 ms. Currently, most early WiMAX deployments are using the TDD duplexing mode. In the future, FDD modes may be used if operators choose to deploy WiMAX in paired cellular spectrum, as is commonly the case in traditional cellular wireless networks.

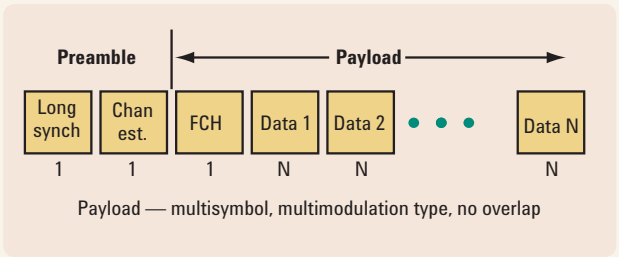

Figure 11. Structure of a fixed WiMAX TDD downlink subframe

Figure 11 shows a generalized view of a fixed WiMAX TDD downlink subframe. The *downlink* subframe begins with two OFDM symbols (QPSK modulation) that are used for receiver synchronization and channel estimation. These two symbols constitute the *preamble*. The preamble is followed by the *frame-control header* (FCH). Within the FCH, the *downlink frame prefix* (DLFP) specifies the type of modulation and the number of symbols associated with subsequent bursts. The data bursts intended for each end user are then transmitted serially.

A short time interval placed between the downlink and uplink bursts is referred to as the *transmit transition gap* (TTG). This is necessary in TDD systems to ensure that the transmission from a base station (the downlink) has ceased before the user terminals begin transmitting data back to the base station (uplink). Similarly, following the last uplink burst, another time interval precedes the subsequent frame and is called the *receive transition gap* (RTG).

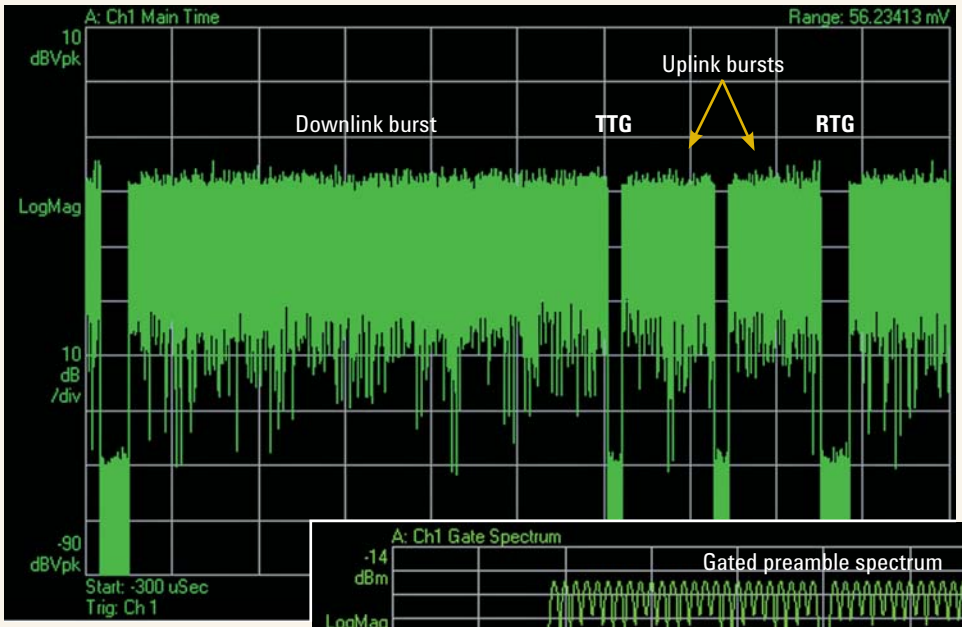

Figure 12. Time response (RF envelope) of a fixed WiMAX TDD frame

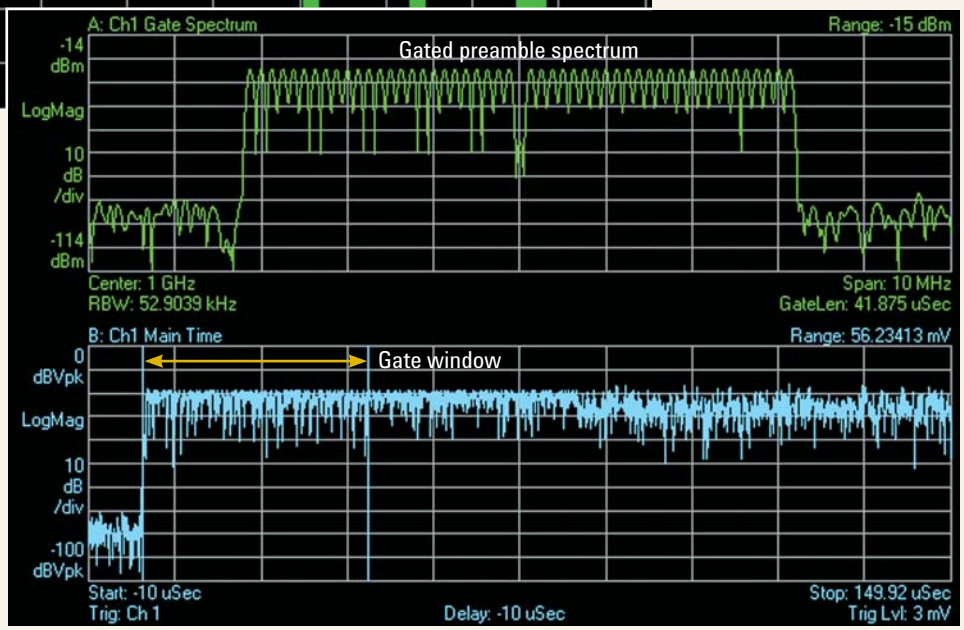

Figure 13. Downlink preamble frequency spectrum (top) and RF power envelope (bottom)

The durations of both gaps are determined by the standard depending on the occupied bandwidth and the OFDM symbol duration. Figure 12 shows the RF power envelope of a WiMAX TDD frame, and the transition gaps are clearly visible.

The data that follow the FCH can vary between 12 and 108 bytes, depending on the modulation type and coding used. In the first symbol of the downlink preamble, not all available subcarriers are used. Rather, only 50 OFDM subcarriers are utilized without occupying the center frequency. In fact, the center frequency (carrier #0) is never transmitted in OFDM schemes to avoid problems with local oscillator (LO) feedthrough (or DC offset in zero-IF designs).[6]

The frequency spectrum of the downlink preamble can be viewed by extracting a segment of the corresponding samples in the time domain using the VSA's time gating feature. This is shown in the upper part of Figure 13 (the 50 active subcarriers are clearly visible). The downlink preamble is transmitted with 3 dB more power than the data in order to facilitate reception, demodulation and decoding of this critical portion of the downlink subframe. Similarly, the uplink frame begins with an OFDM symbol, which the base station uses to synchronize with the user terminal.

Conclusion

With roots that reach back to the early 1930s, OFDM has helped enable a wide range of existing and emerging communication technologies. By dividing data transmissions across a series of closely spaced orthogonal subcarriers, OFDM enables greater transmission efficiency in real-world radio environments.

OFDM can be used with an adaptive choice of modulation and coding schemes, favoring either transmission speed when LOS visibility is available or transmission reliability in the case of NLOS and the presence of channel disturbances such as fading.

Looking to the future, the original 802.16-2004 fixed WiMAX standard has evolved to support mobility with the advent of mobile WiMAX (see sidebar). This approach leverages OFDM and adds enhancements that support mobile applications and multiplexed parallel access by end users and the constantly changing paths, time delays and frequency shifts that occur when wireless equipment is in motion.

References

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Additional information regarding WiMAX measurements is available at www.agilent.com/find/wimax.

Mobile WiMAX: 802.16e-2005 OFDMA

Recently, strong interest has developed around IEEE 802.16e, an amendment to the original fixed WiMAX standard. Often called OFDMA or mobile WiMAX, the amendment enables multiple users to share the available spectrum in parallel for both downlink and uplink (fixed WiMAX supports only serial access based on time-slot allocations). Most importantly, mobile WiMAX supports mobility by allowing handoffs from one cell to the next without breaking the IP connection.

Fixed WiMAX is based on a 256-carrier FFT, and only 200 of the possible 256 carriers are actually used. Of the 200 carriers, 192 of these are used for data and eight are used as pilots. OFDMA adds more flexibility in the available number of pilots and subcarriers. Four different FFT sizes are available: 2048, 1024, 512 and 128. These can be used with bandwidths ranging from 20 MHz down to 1.25 MHz; the FFT size changes based on the bandwidth, retaining subcarrier spacing

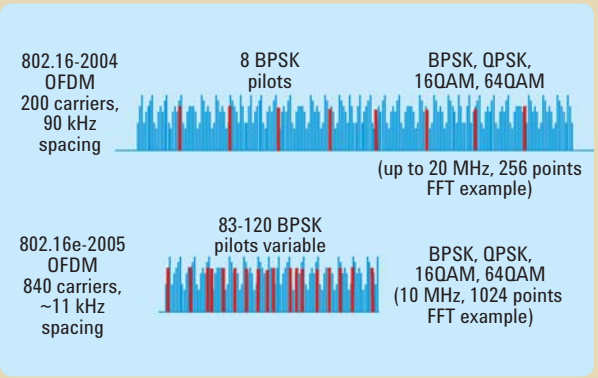

Figure A. Contrasting OFDM implementations: fixed and mobile WiMAX

of about 11 kHz. The number and location of BPSK pilots is variable, and they are not evenly spaced. The number of subcarriers, number of FFT points and spacing of subcarriers is determined by the certification profile supported by a particular system.

Improving

Improving Spectrum Measurement and Monitoring in Commercial Wireless Applications

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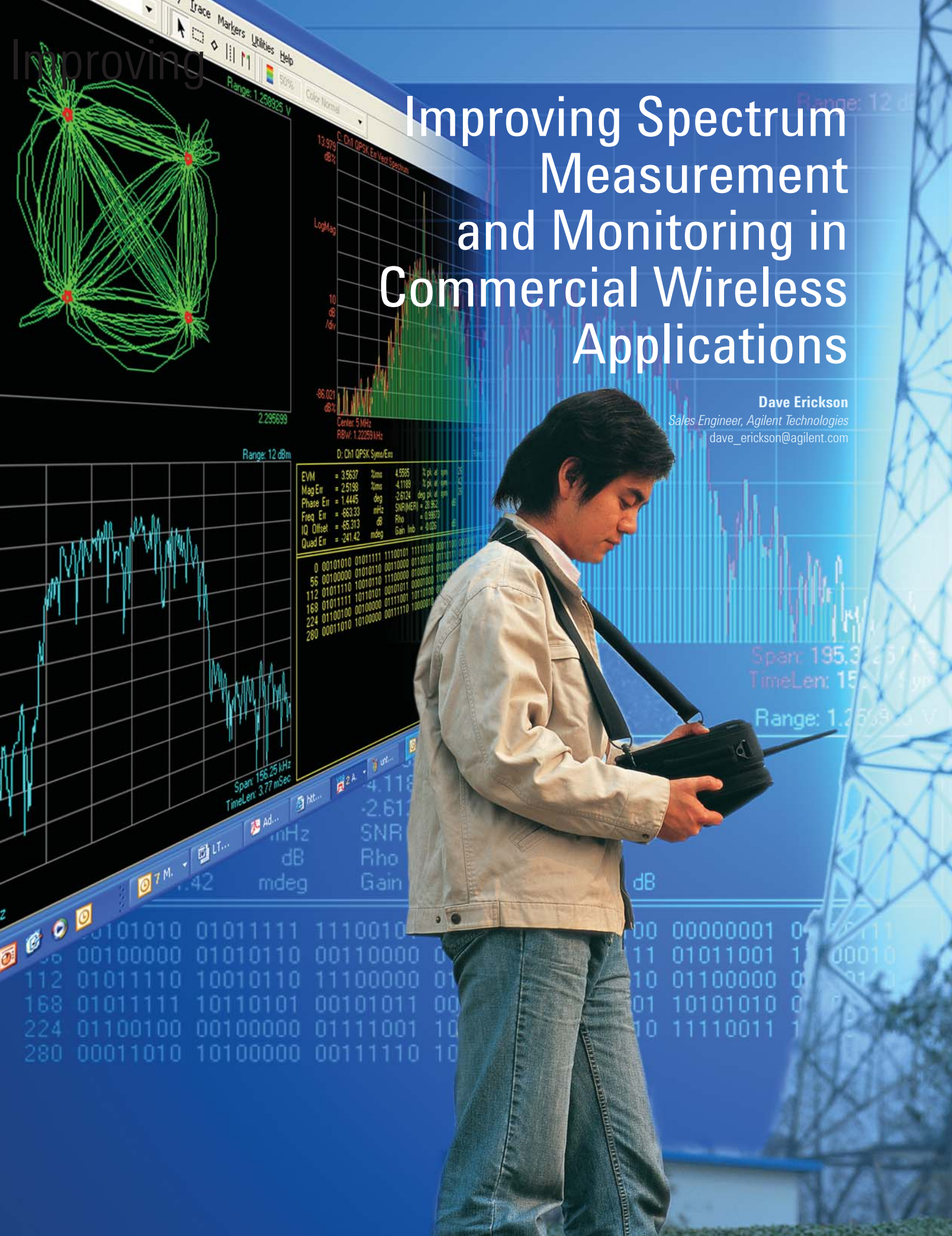


After recognizing the market value of the available frequency spectrum, many governments around the world began auctioning the right to use their airwaves. Companies that purchased or licensed spectrum rights are offering a wide range of for-fee services — voice calls, text messaging, wireless Internet, satellite radio, HDTV and even TV via cell phone. For service providers and equipment manufacturers, substantial sums of money are at stake in the creation and delivery of wireless products and services. Money is also at risk in the form of fines for improper use — intentional or unintentional — of regulated frequency spectrum.

In the realm of unlicensed spectrum, numerous equipment manufacturers offer widely used products such as cordless phones and wireless Internet-access devices. These manufacturers are responsible for ensuring their devices deliver high performance and meet the applicable standards and regulations.

As a result, the past decade has seen tremendous growth in the need for spectrum measurement and monitoring. In commercial applications, spectrum measurement is used to verify and troubleshoot wireless services and systems. Spectrum monitoring is used to identify sources of interference and detect changes in the environment that may degrade system performance.

The entire wireless industry relies on spectrum measurement and monitoring, from service providers to equipment manufacturers to installation and maintenance organizations. While the industry has diverse requirements that span actual and simulated measurements, all participants share the need to understand signal coverage and identify interference sources.

Effective measurement and monitoring

Many subtle issues affect measurement results. Fortunately, off-the-shelf tools and common techniques provide useful information that helps enhance the quality, reliability and cost of wireless products and services.

The heart of every solution is a measurement receiver that must address several key needs. For example, the Agilent E6474A wireless network optimization platform is designed for installation and maintenance of cellular phone systems, providing key measurements required by the cellular industry (Figure 1). In contrast, spectrum analyzers and vector signal analyzers (VSAs) are used for general-purpose wireless spectrum monitoring applications.

Figure 1. The Agilent E6474A quickly and accurately identifies problems in wireless voice and data networks.

The key to selecting a suitable measurement receiver is identifying the essential specifications that address the target application. Specific wireless standards have requirements that range from modest (Bluetooth®) to very demanding (GPS). These requirements translate into performance specifications such as noise figure and third-order-intercept (TOI), and into features such as built-in "personalities" that provide standards-compliant measurements of wireless formats.[1]

Comparing general-purpose analyzers

While traditional spectrum analyzers measure only signal amplitude, VSAs measure amplitude and phase. This enables measurements of digitally modulated signals, which often vary in amplitude and phase over time. VSAs can also measure error vector magnitude (EVM), a calculated value that describes the quality of a digitally modulated signal, similar to measuring distortion of an analog modulated signal (Figure 2).

VSAs also can measure signal fading, which is caused by reflections of wireless signals off objects between transmitting and receiving antennas. Depending on the pathways and time delays of the reflections, the reflected power may add or subtract from the power in the direct path. This becomes more complex when wireless equipment is in motion — such as a cellular phone in a moving car — and the paths, time delays and frequency are constantly changing. Such measurements are also used to create or verify fading models, which help assess the usefulness of a wireless technology in a given operating environment.

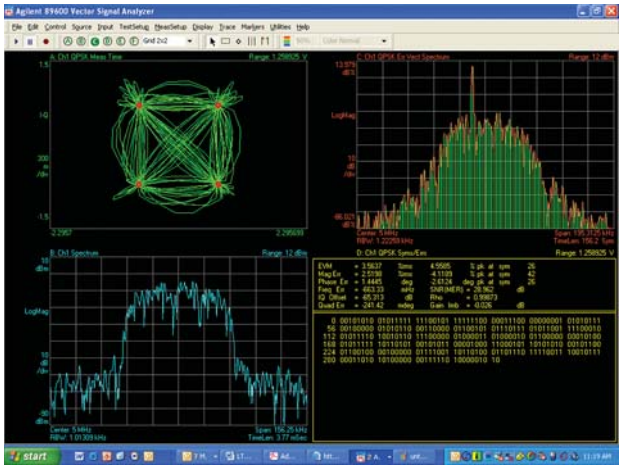


Figure 2. EVM is an important quantitative measure of digitally modulated signals.

Measuring signal coverage

In-band signal strength is a key measure of performance for any wireless service. Several factors make it difficult to accurately measure low-power wireless signals: their low power level, fading, strong out-of-band signals and their noise-like nature.

Accurate assessment of low-power signals requires a measurement receiver with a low noise figure. This value determines the minimum signal power that the measurement receiver can detect; the lower the noise figure, the greater the ability to measure weak in-band signals. As an example, accurate outdoor measurements of a CDMA2000 base transceiver station (BTS) require a measurement receiver with a noise figure of less than 4 dB. High-performance spectrum analyzers have on the order of 12 dB noise figure with no input attenuation. Fortunately, the addition of an external low-noise amplifier (LNA) to the analyzer input will improve noise figure performance.

1. Noise figure is a calculation of the noise a measurement receiver adds to measured signals. TOI is a calculation that determines how strong an input signal can be without significantly distorting desired signals.

Accurately measuring low-power signals in the presence of high-power signals requires a measurement receiver with adequate TOI performance. Filtering is required to limit the bandwidth at the input in the measurement receiver, removing strong out-of-band signals that may cause in-band, co-channel, nonlinear distortion in the measurement receiver. High-performance spectrum analyzers have on the order of 19 dBm TOI with no input attenuation.

If an LNA is added to the input of the measurement receiver, it also must have good TOI performance. LNAs with high TOI can generate high output power levels; the addition of a power limiter between the LNA output and the measurement receiver input will prevent inadvertent damage to the input circuitry. Adding isolators will improve the overall input impedance match with external antennas and other components, minimizing variations in frequency response that degrade power measurement accuracy.

Accurate measurements of in-band signal power are important when verifying system coverage requirements or when validating propagation and system planning models. High-performance spectrum analyzers have on the order of ±1.5 dB absolute power accuracy. Low phase noise performance in the measurement receiver is also important when measuring narrowband signals.

Fading causes amplitude variations that affect power measurements, and narrowband signals such as APCO-25 are more susceptible to inaccuracy in power measurements. To improve accuracy, multiple measurements must be made at different locations determined by center frequency and environment. It is then possible to estimate the true power based on knowledge of the fading characteristics. If the fading characteristics are not known, they can be measured using a VSA or channel sounder.

Measuring and monitoring interference

Interference — whether intentional or unintentional — will degrade wireless system performance. Before system deployment, interference measurements can be used to determine optimum placement of wireless equipment. After installation, interference detection and monitoring can be used to help troubleshoot and resolve system problems.

A highly flexible measurement receiver simplifies capture of elusive interfering signals. For example, the ability to adjust parameters such as sweep speed, measurement bandwidth and detector type can accelerate the identification of interfering signals. The ability to change external components (e.g., LNAs, filters, antennas) under computer control accelerates the search for unwanted signals. These capabilities are needed to identify four common causes of interference: the power in adjacent and alternate channels, co-channel interference, intermodulation distortion (IMD) and blocking.

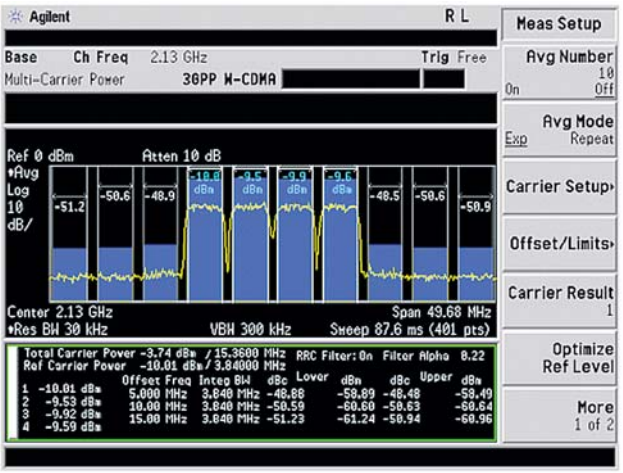


Figure 3. ACP measurements can help identify interfering signals above or below an assigned frequency channel.

Adjacent/alternate channel power (ACP): One key source of interference is receiver distortion caused by wireless signals that operate above or below an assigned frequency channel. Measuring adjacent and alternate power is easy due to the high power levels of the adjacent and alternate signals that create potential interference in wireless receivers (Figure 3). Low phase noise in the measurement receiver can improve ACP measurement accuracy.

Co-channel: Another important source of interference is a signal transmitted at the same frequency as the desired signal. This form of interference may occur when a frequency band is being cleared for a new service, when equipment malfunctions, or when another operator is transmitting improperly. It may also appear to be present if distortion is affecting the measurement receiver. Co-channel interference is difficult to measure because its characteristics are unknown, its bandwidth will vary, and it also may be intermittent, low-power or pulsed. A versatile measurement receiver simplifies characterization of co-channel interference.

IMD: In a wireless receiver, the nonlinear interaction of two or more strong signals can create a co-channel interfering signal. Fortunately, the strong signals that create IMD are easy to measure due to the high power level of the signals. While it is easy to identify the contributing frequencies when only two signals are present, the presence of three or more strong signals can also cause IMD. Estimating the extent of co-channel IMD becomes exponentially more difficult as the number of signals increases. A wideband frequency sweep followed by post-processing of the data will reveal the signals generating co-channel IMD.

Blocking: A very strong signal can penetrate the shielding or filtering in a wireless receiver; however, its high power level makes it easy to measure. The search for blocking signals relies on wideband sweeps, which can take a long time when trying to detect intermittent signals with unknown characteristics.

Isolating sources of interference

The most common interfering signals carry amplitude modulation or frequency modulation (AM or FM); however, as wireless technologies evolve, it is becoming more likely to experience interference from digitally modulated signals.

When determining the source of interference, one key question must be answered: Is the interference intentional or unintentional? Intentional interference could be an adjacent-channel signal from a BTS for a user that is much further away. If the interference is intentional, it can often be mitigated to maintain system performance, which might include adjustments to existing equipment, the addition of new equipment, the deployment of higher-performance equipment or an upgrade to newer technology.

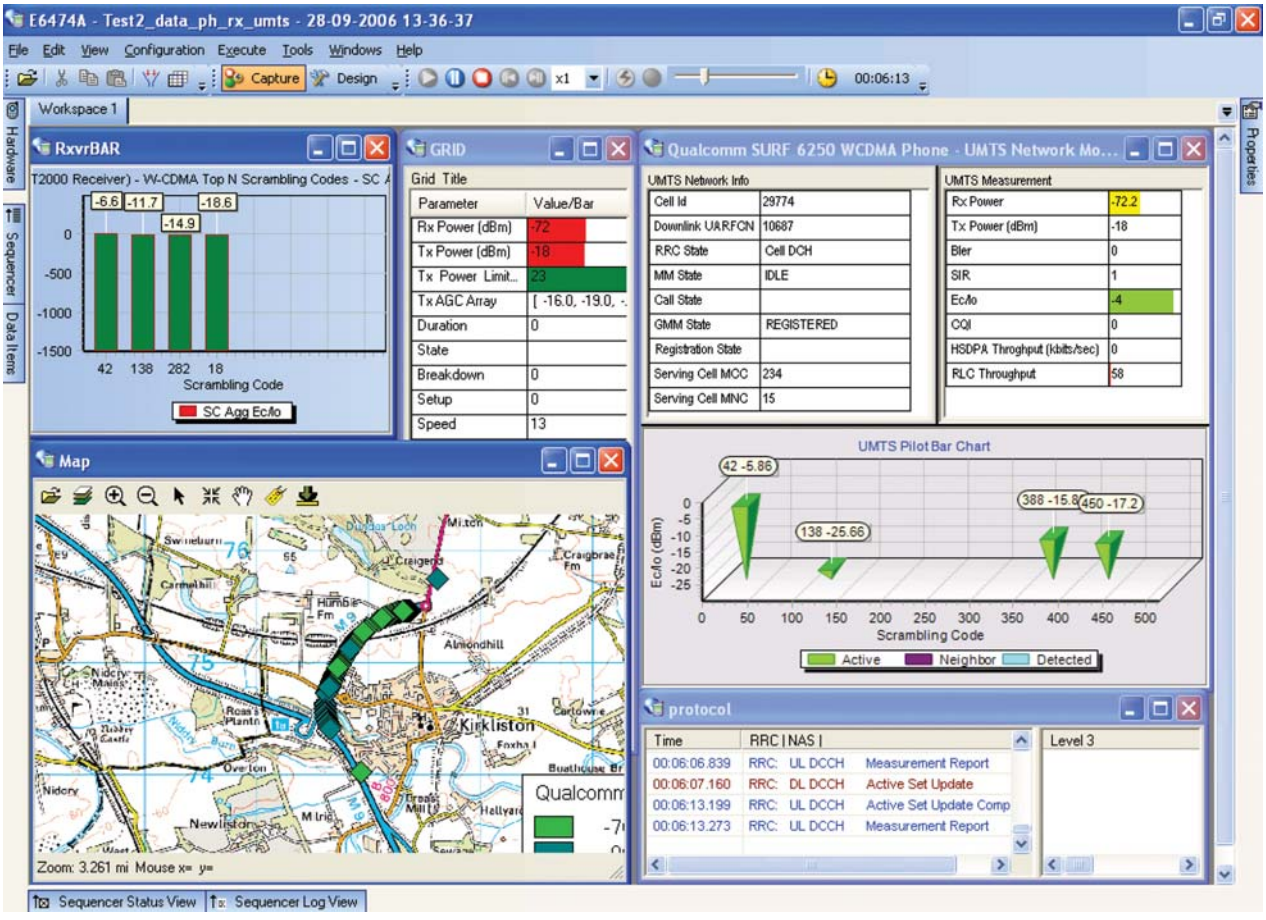


Figure 4. Maps and geolocation information can help pinpoint sources of interference.

Unintentional interference may come from a malfunctioning transmitter or a newly activated transmitter (e.g., terrestrial HDTV). If the source of interference is unintentional, the interferer must be quickly found and informed.

Determination: The source of interference can often be determined if the measurement receiver can demodulate the interfering signal. For AM and FM signals, the bandwidth can be measured and compared to known services such as TV, AM/FM radio, trunked radio and so on. Many measurement receivers have AM and FM tuners with audio outputs, enabling the operator to listen to the transmission and identify the source. Through regulatory databases, it may be possible to identify the owner and remedy the problem.

For digitally modulated signals, it takes time to determine modulation type, symbol rate, filtering and so on. Once the modulation characteristics are identified, they may be enough to determine the technology being used and, through a regulatory database, identify and inform the owner.

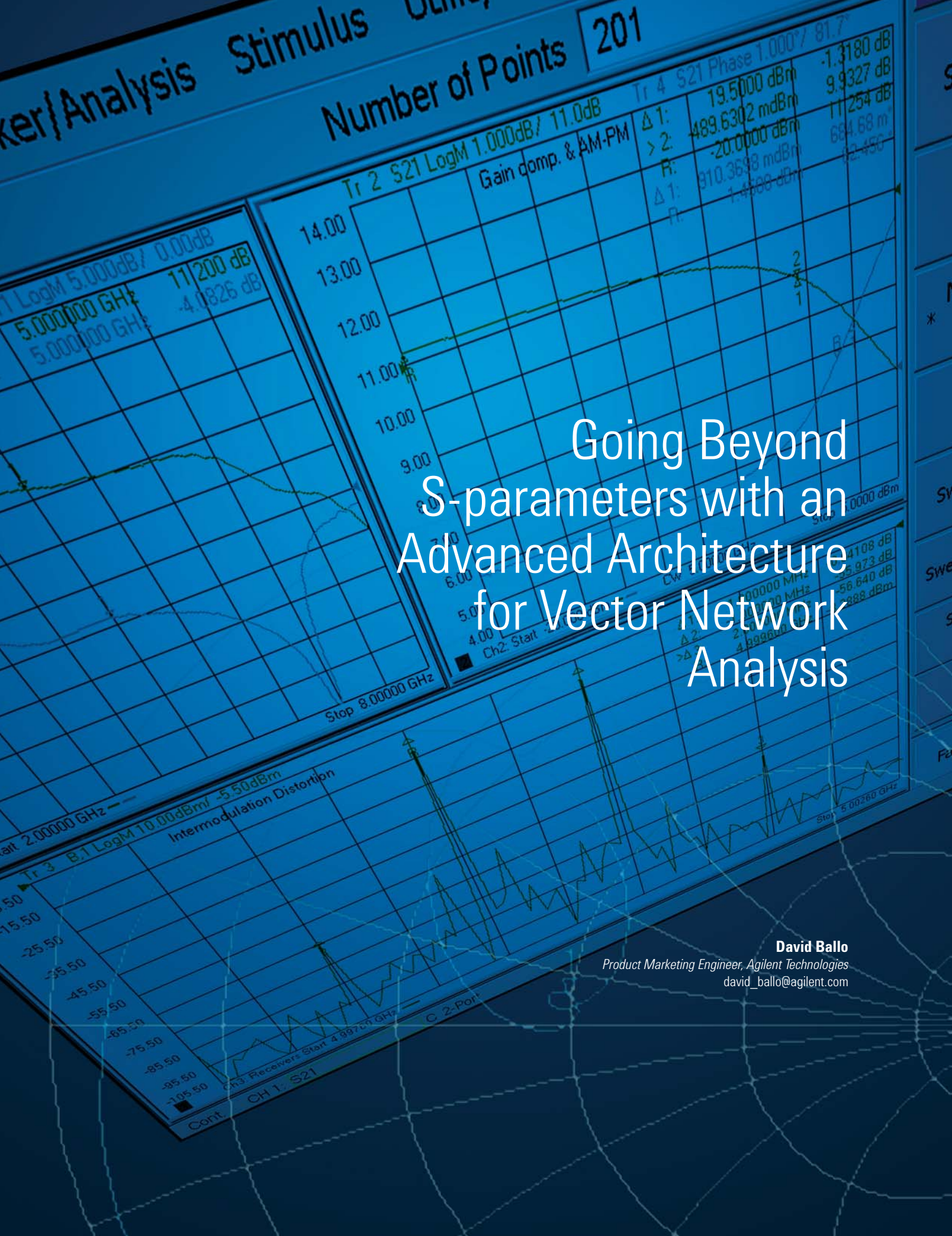
Direction: The source of interference can be found using a mobile measurement receiver and directional antenna, which has higher gain in a specific direction. Rotation of the antenna will cause a noticeable variation in the power level of the interference, and will provide a bearing to the source of interference. The use of multiple measurement receivers equipped with directional antennas enables triangulation to the interfering emitter.

Mapping: It is often useful to complement coverage and interference measurements with geolocation data. For example, a database of licensed transmitters with propagation models can be overlaid with measurement and topography data to determine if propagation models are correct or if specific transmitters are interfering with a wireless service (Figure 4).

Conclusion

Carriers and equipment manufacturers have invested large sums of money in the products and services that enable present and future wireless services. Companies that utilize advanced spectrum measurement and monitoring tools (Figure 5) will be better able to deliver higher quality products and services with greater reliability and at lower cost. The likely results are improved customer satisfaction, a greater return on investment and enhanced revenue growth.

Figure 5. Designed for field use, the N9340A handheld RF spectrum analyzer provides exceptional performance for highly portable spectrum-monitoring applications.



Going Beyond S-parameters with an Advanced Architecture for Vector Network Analysis

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In both R&D and manufacturing, engineers face a number of significant challenges when testing radio frequency (RF) components. In R&D, solving design challenges faster and with fewer design iterations is paramount. Manufacturing demands ever-lower test times and test costs, while maintaining accuracy and maximizing yield.

One way to ease the pressure is with a flexible, highly integrated measurement solution such as the Agilent N5242A PNA-X microwave network analyzer. With its advanced architecture, the PNA-X not only delivers excellent performance and accuracy, but it also can be configured for a variety of measurements beyond the traditional scattering parameters (S-parameters) associated with network analyzers. Built-in elements such as a second signal source and frequency combiner enable accurate, informative characterization of nonlinear behavior in RF and microwave devices, particularly amplifiers, mixers and frequency converters.

Ensuring accurate system simulation

Accurate magnitude and phase measurements are crucial to modern wireless and aerospace/defense systems. During the design phase, system simulations need highly accurate component characterizations to ensure that the system will meet its performance requirements. In manufacturing, accurate measurements verify that each component meets its published specifications.

S-parameters are the most widely used measurements of RF components — filters, amplifiers, mixers, antennas, isolators and transmission lines. These measurements characterize the complex-valued (magnitude and phase) reflection and transmission performance of RF devices in the forward and reverse directions. They also fully describe the linear behavior of RF components, which is necessary, but not sufficient, for full-system simulation. Deviations such as non-flat amplitude response versus frequency or non-constant-slope phase response versus frequency can cause serious system degradation.

System impairments also result from the nonlinear performance of some RF components. For example, amplifiers exhibit gain compression, amplitude-modulation-to-phase-modulation (AM-to-PM) conversion and intermodulation distortion (IMD) if driven at power levels that exceed their linear range.

Outlining the core measurements

The most commonly used instrument to characterize RF components is the vector network analyzer (VNA). A traditional VNA contains a single RF signal generator that provides a stimulus for the device under test (DUT) and multiple measurement receivers to measure incident, reflected and transmitted signals in both the forward and reverse directions (Figure 1). The source sweeps in frequency at a fixed power level to measure S-parameters and sweeps its power level at a fixed frequency to measure amplifier-gain compression and AM-to-PM conversion. These measurements characterize linear and simple nonlinear device performance.

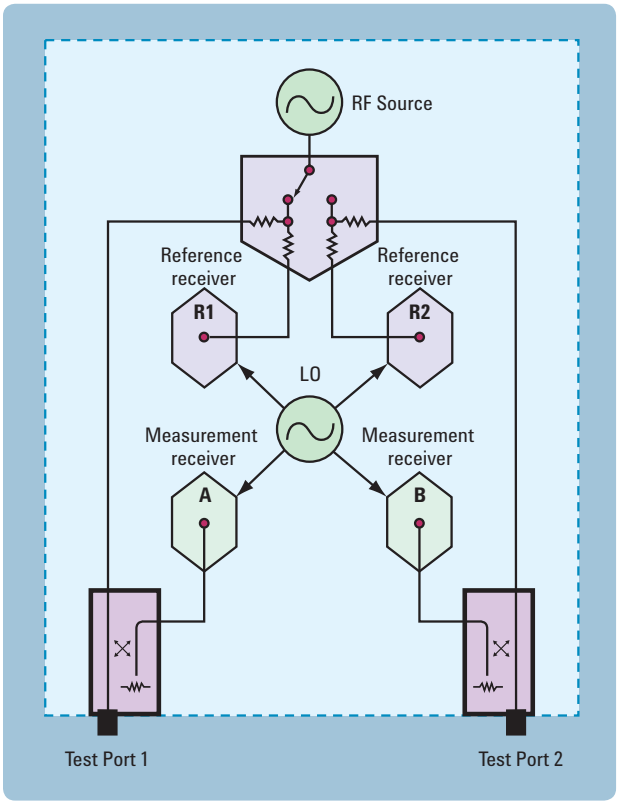

Figure 1. Block diagram of a traditional two-port VNA

For basic S-parameters and compression testing, the source and receivers are tuned to the same frequencies. By offsetting the source and receiver frequencies, however, amplifier harmonics can be measured by tuning the receivers to integer multiples of the stimulus frequency. The ability to offset the source and receiver frequencies also enables measurements of magnitude, phase and group-delay performance of frequency-translating devices such as mixers and frequency converters.

While these measurements are typically done with a continuous-wave (CW) stimulus, many devices require testing with a pulsed-RF stimulus, which means the test signal must be gated on and off with a specific pulse width and repetition rate.

Traditional VNAs have two test ports, which was sufficient when most RF devices had only one or two ports. With the rapid rise of wireless communication, three- and four-port devices have become commonplace, and as a result, two- and four-port network analyzers are equally prevalent.

Simplifying amplifier and mixer measurements

Available with two or four ports, the PNA-X features four major improvements to the traditional VNA architecture:

- **Two sources:** Frequency and power level settings for the second internal source are independent from those of the main source. The second source can be used for nonlinear amplifier tests such as intermodulation distortion (IMD) or as a fast, local oscillator (LO) signal for testing mixers and converters.
- **Signal combiner:** The internal signal combiner can sum the two sources prior to the associated test-port coupler of the instrument. This simplifies the setup of amplifier tests that require two signal sources.
- **Switching and access points:** Additional switches and RF access points enable flexible signal routing and the addition of external signal-conditioning hardware (e.g., a booster amplifier) or external test equipment (e.g., a digital signal generator or vector signal analyzer).
- **Pulse capabilities:** Internal pulse modulators and pulse generators provide a fully integrated pulsed S-parameter solution.

These improvements simplify test setups and improve test times when measuring amplifiers, mixers and converters. They also work together to expand the range of measurements that can be made with a single set of connections to the DUT. Figure 2 shows an example of simultaneous measurements of S-parameters, gain and phase compression and fixed-signal IMD on an amplifier.

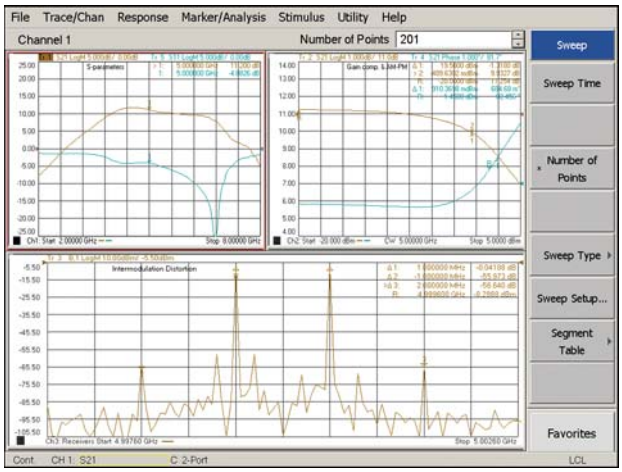

Figure 2. PNA-X example showing simultaneous measurements of amplifier S-parameters, compression and IMD

Enhancements in both sources also simplify amplifier and mixer measurements. For example, the maximum signal power available at the test ports is typically +13 to +20 dBm (depending on model and frequency). This is very useful for driving amplifiers into their nonlinear region and is often required when using a source as an LO signal for testing mixers. The sources also contain low harmonics (typically –60 dB or better), which improves harmonic and IMD measurement accuracy. Also, a power sweep range of typically 40 dB makes it easier to characterize an amplifier's transition from linear to nonlinear operation.

Addressing a variety of measurements

While a VNA needs just a single RF source to measure S-parameters, compression and harmonics of components, a second internal source enables complex nonlinear measurements such as IMD, especially when coupled with a signal combiner.

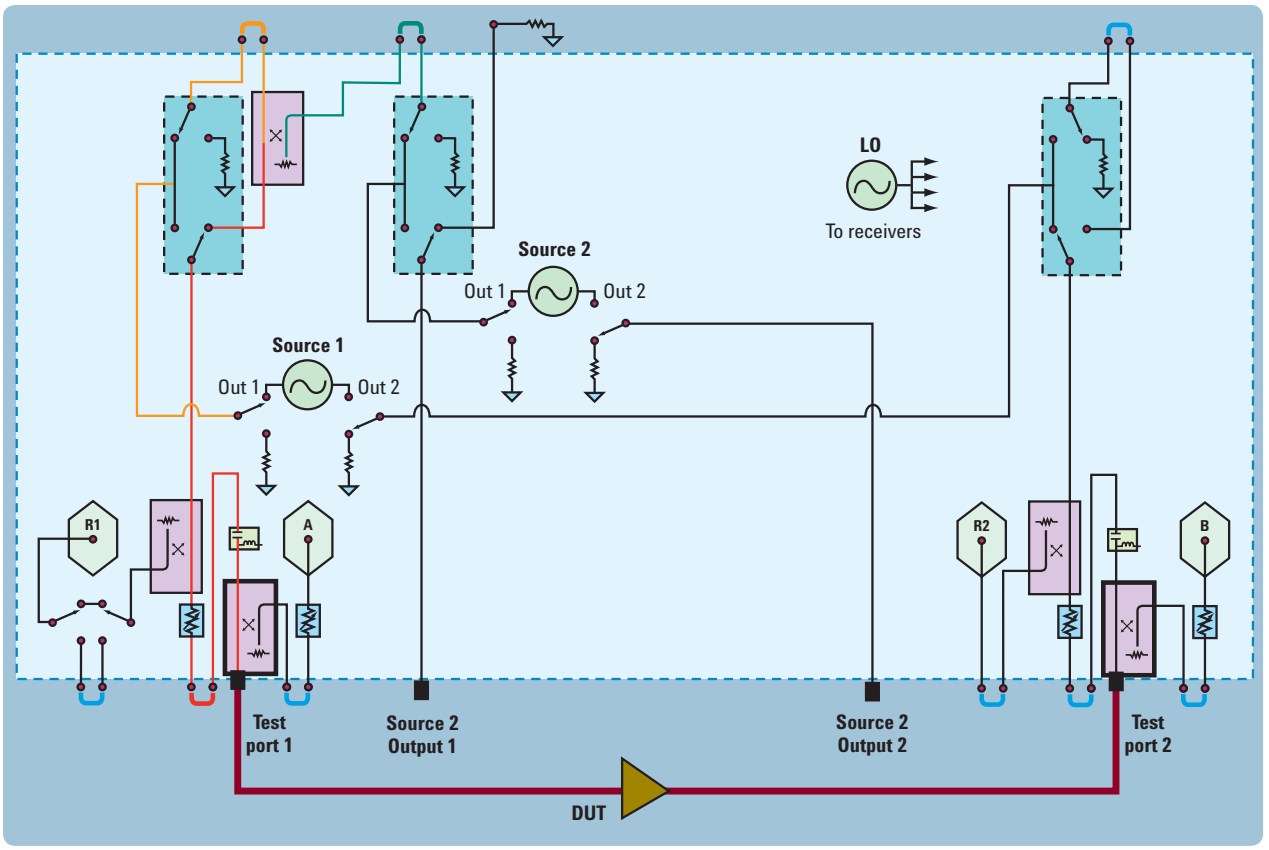

Figure 3. Block diagram of a two-port PNA-X configured for IMD measurements

For IMD measurements, two signals are summed using the signal combiner and then routed to the input of an amplifier under test (AUT). Figure 3 shows how the PNA-X accomplishes this with the internal sources and combiner.

AUT nonlinearities will cause intermodulation products to appear alongside the amplified input signals. In communications systems, these unwanted products fall within the operating band and cannot be removed by filtering. In practice, only the third-order products are measured because they are the most significant contributors to system impairment.

Figure 4 shows an example of a swept IMD measurement performed with the PNA-X. The two middle traces show the stimulus signals and the two lower traces show the IMD products. The upper trace takes advantage of the PNA-X's equation feature to calculate and display the third-order intercept point (IP3).

Figure 4. PNA-X example of a swept-frequency IMD measurement

A useful variation of swept IMD is to sweep power levels rather than frequencies. This helps R&D engineers develop nonlinear, behavior-based models of transistors and amplifiers. Figure 5 shows such a measurement: Both the amplitude and phase of the fundamental plus third-, fifth- and seventh-order intermodulation products are shown versus input power.

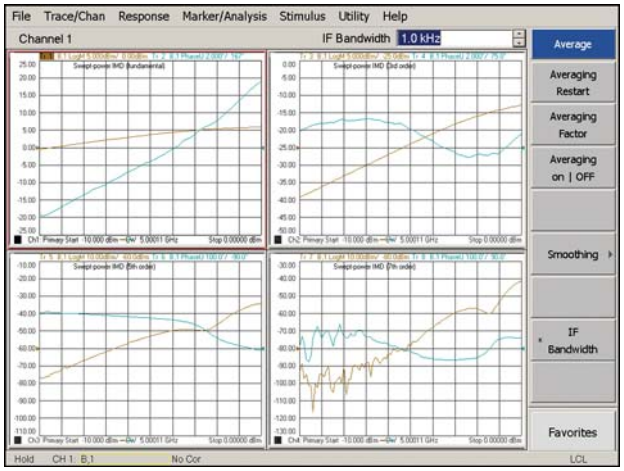

Figure 5. PNA-X example of a swept-power IMD measurement

Using a VNA for these measurements offers three advantages over other approaches. First, a single test instrument and a single set of connections can produce a full suite of measurements: S-parameters, gain compression, output harmonics, IMD and so on. Second, with the VNA's power-meter-based calibrations, measurement accuracy is higher than that obtained using a spectrum analyzer. Finally, this measurement would take several minutes using a spectrum analyzer and two standalone signal generators, but only takes about 0.6 second on the PNA-X.

Phase-versus-drive is another common two-source test easily accomplished with the PNA-X. This parametric test characterizes an amplifier's small signal performance in the presence of a large adjacent-channel or out-of-band signal. One large signal and one small signal, each at different frequencies, are summed and delivered to the AUT; the power of the large signal is varied (using a power sweep) while the S21-phase of the smaller signal is measured.

Another two-signal technique used to develop nonlinear, behavior-based transistor and amplifier models is called "hot S-parameters." This method characterizes the small signal S-parameters of an amplifier (or often, just S22) at a given frequency in the presence of a large (hot) input signal that is offset from the S-parameter test signal and that drives the AUT output into compression. Care must be taken to ensure that the hot signal coming out of the AUT is not greater than the damage level of the VNA.

Measuring balanced components

Balanced circuitry reduces susceptibility to, and generation of, electromagnetic interference. Balanced components may be balanced-to-single-ended devices with three RF ports or balanced-to-balanced devices with four ports. Testing these components is easy with a four-port VNA, which can measure differential- and common-mode responses as well as mode-conversion terms.

These tests can be accomplished with either a single-ended or true-mode stimulus. The single-ended method tests one port of the DUT at a time (requiring just one RF source) and mathematically calculates the differential-, common- and cross-mode behaviors. This is the fastest and most accurate technique provided the applied power levels keep the AUT in a linear or mildly compressed region of operation.

Testing the balanced performance of an amplifier under high-drive-level conditions, in which nonlinearities cause significant errors in single-ended measurements, requires a true-mode stimulus. This method applies two signals of equal amplitude to the input terminal pair of an amplifier with a phase difference of either 180 degrees (the differential-mode signal) or zero degrees (the common-mode signal). Conceptually, this is easily done with a dual-source VNA, but two things are required for accurate measurements: high-resolution adjustment of phase difference between sources and the ability to adjust source phase and amplitude to offset input mismatch caused by the interaction of source output impedance and AUT input impedance. The PNA-X meets both of these requirements.

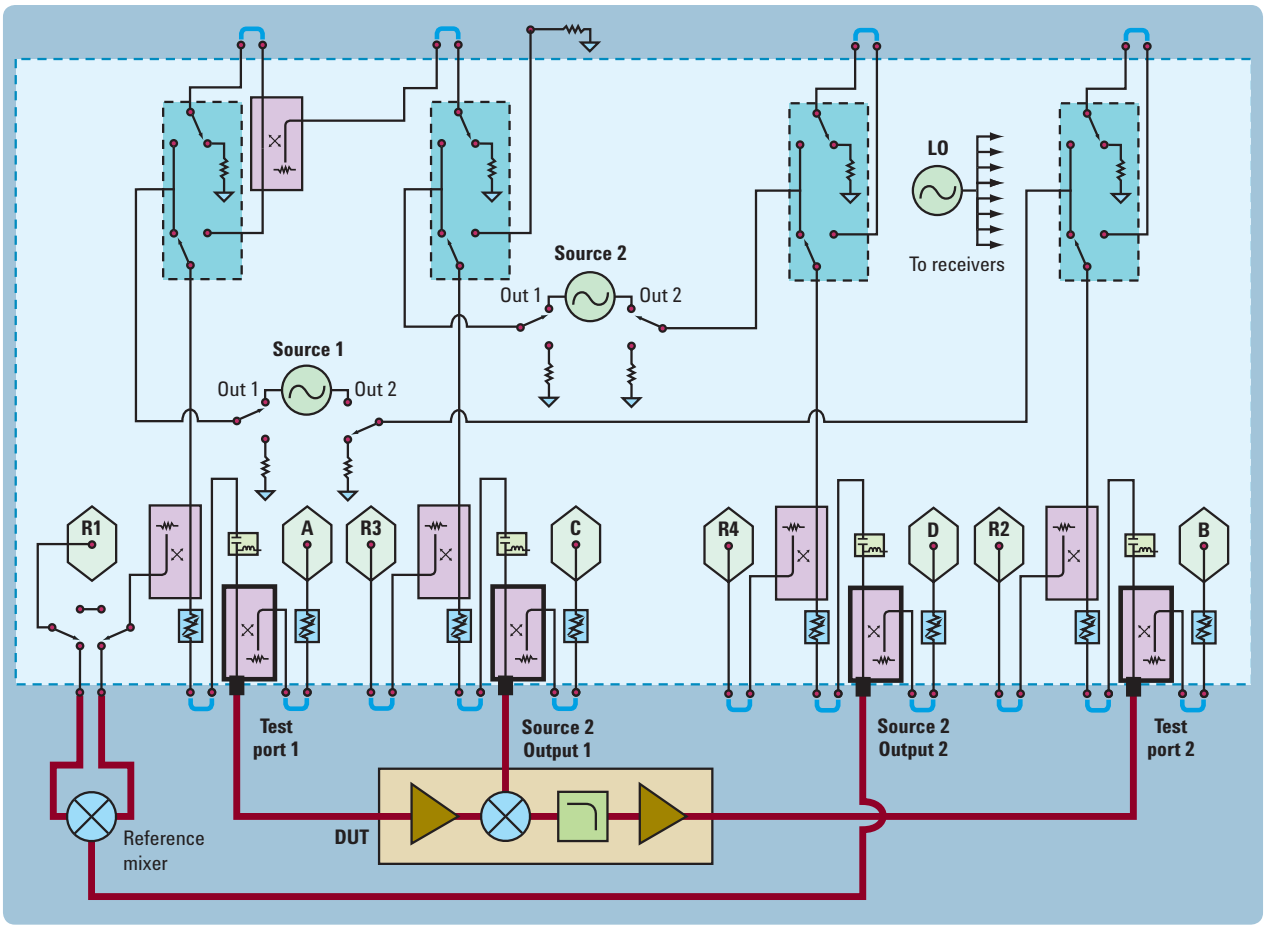

Figure 6. Block diagram of a four-port PNA-X configured for vector-mixer measurements

Testing mixers and converters

A second internal source is also useful for testing frequency-translating devices such as mixers or converters, which require an LO signal in addition to an input stimulus. The second source is especially useful for swept-LO testing, where the LO signal is swept in conjunction with the RF input signal but with a fixed offset. This approach is often used to measure the front-end components in broadband frequency converters. Using an LO signal derived from a VNA's internal source provides considerable speed improvements when compared to using an external signal generator (up to 35 times faster with the PNA-X).

The setup for mixer and converter measurements using the PNA-X is very simple. To test port match and conversion loss or gain, the input, output and LO ports of the DUT are connected to ports one, two and three, respectively, on the PNA-X. Adding a reference mixer enables testing of the phase or group-delay response of a mixer or converter. The dual-outputs of the second source can be used to drive both the reference mixer and the DUT mixer (Figure 6).

Conclusion

VNA-based test systems provide the engine for measuring RF and microwave components used in wireless communication and aerospace/defense systems. Compared to traditional VNAs, the advanced architecture of the Agilent PNA-X microwave network analyzer provides greater flexibility, enabling engineers to measure a broad range of high-performance, leading-edge components with a single set of connections. The key additions are the second signal generator and an internal signal combiner, which simplify measurements of amplifiers, mixers and converters. In addition to traditional single-source measurements of S-parameters, compression and harmonics, the two sources can be used in IMD, phase-versus-drive, hot S-parameter and true-mode stimulus testing. The attributes of high port power, low harmonics and wide power-sweep range are well-matched to the requirements of today's devices.

Applying a Flexible Solution for Millimeter-Wave Measurements

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Between 30 and 300 GHz, the number of applications that millimeter-wave measurements are used for is increasing. From high data rate to automotive to radio astronomy, the benefits of a flexible measurement solution are becoming more apparent. Across these applications, millimeter-wave measurement solutions must address many disciplines such as device characterization on wafers in a probing environment, or module testing with either waveguide or coaxial interfaces. Solutions also can include measurements of materials that are either in fixtures or over free space, or testing of antennas that are either in open range or chambers.

Compared with applications below 3 GHz, today's demand is relatively low for millimeter-wave components, but the expected performance is quite high. Consequently, a measurement solution with an extendable frequency range and expandable measurement capabilities will provide much greater flexibility to suit multiple applications.

In many emerging electronic technologies, the first components — devices that are fabricated on wafers, for instance — are the basic building blocks. These devices are then diced and wire-bonded into circuits, eventually evolving into highly integrated modules characterized by increasing functionality packed into an ever-smaller footprint. Devices are first characterized on-wafer before being further tested as modules. Data obtained while testing these devices on-wafer are used for parameter extraction in order to build models, which can then be used for circuit simulations.

Making millimeter-wave measurements

Building accurate models for circuit simulations requires high-quality, 220-GHz probing solutions. For example, Figure 1 shows on-wafer measurements for 50-nm T-gate metamorphic GaAs HEMTs from 140 to 220 GHz.[1] All four S-parameters are available for viewing simultaneously. Looking at the lower left trace, S21 crosses the x-axis at about 150 GHz, the F_t of the transistor. To reveal the true gain of the device, a de-embedding process is required using an .s2p file (raw data), which can be performed either inside the network analyzer or offline.

Measurements were made using an Agilent N5250A PNA Series millimeter-wave network analyzer with 140 to 220 GHz (N5260AW05) test-head modules configured for on-wafer measurements with the Cascade Microtech Summit 12K probe station (Figure 2, which shows the 110-GHz version of the system). The full two-port on-wafer calibration performed was line, reflect, reflect, match (LRRM) using Cascade Microtech's WinCal 2006 calibration software.

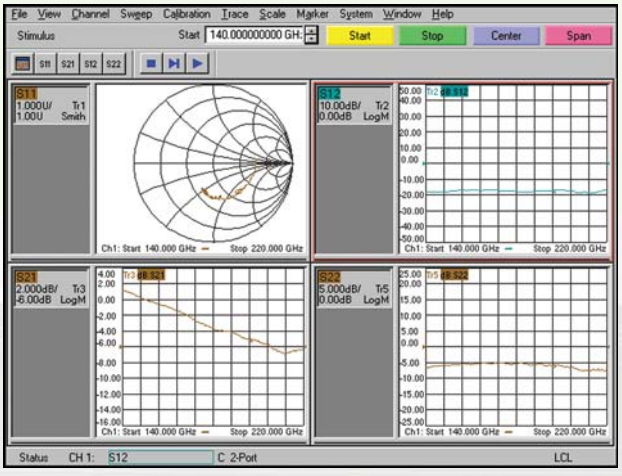


Figure 1. On-wafer measurements of 50-nm T-gate metamorphic GaAs HEMTs show all four S-parameters on a single display.

1. Devices were fabricated and measured by Dr. Khaled Eqaid, Dept. of Electronics, University of Glasgow.

Figure 2. N5250A 110 GHz millimeter-wave system with Cascade Microtech's Summit 12K probe station. Inset shows Cascade Infinity Probe (GSG 150), waveguide versions to 220 GHz.

By adding a modulator (Agilent Z5623AH81) and a dual-output pulse generator (Agilent 81110A), the same equipment was transformed into a solution for pulsed measurements. Figure 3 shows a pulse-profiling measurement for a simple through device at W-band, 75 to 110 GHz. The pulse setup used for these measurements is as follows:

- Pulse repetition interval (PRI): 4 µs
- RF pulse width (PW): 2 µs (50% duty cycle); PW can be as narrow as 20 ns
- B receiver gated pulse width: 20 ns (0.5% duty cycle)
- Measurement frequency: 100 GHz

Pulse profiling is a very useful analysis tool because it reveals any distortion of the pulse caused by the device under test (DUT). This is done by stimulating the DUT with a pulsed signal at the input and then retracing the signal at the output to identify changes in the pulse shape. Any such changes would imply non-ideal (e.g., nonlinear) behavior of the DUT.

Modifying the system to cover a different millimeter-wave frequency band is as easy as changing the test-head modules. For example, replacing the N5260AW05 (140 to 220 GHz) module with the N5260AW03 will shift the frequency band to 220 to 325 GHz. Improved system dynamic range or trace noise above 200 GHz is easily achieved by adding two external synthesizers such as the Agilent PSG signal generators. Each synthesizer would be configured with Option 520 for 20 GHz coverage; one would provide the RF signal and the other the local oscillator (LO).

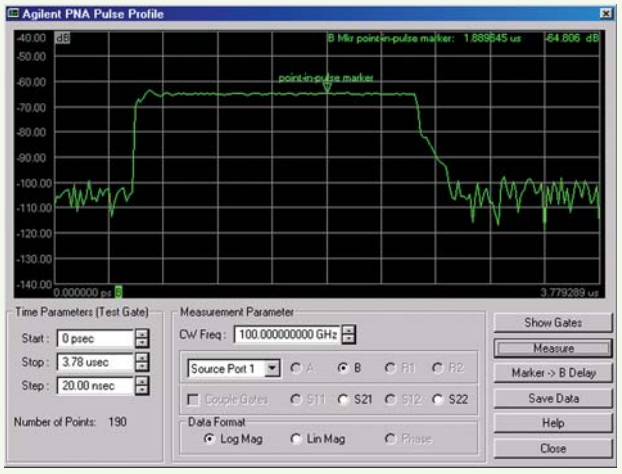


Figure 3. Pulse-profiling measurements will reveal distortion caused by nonlinear behavior of the DUT.

The same equipment setup can also be used to perform related measurements such as average pulse, point-in-pulse and pulse-to-pulse. This configuration also lends itself to indoor antenna measurements, which use pulsed millimeter-wave techniques to gate out unwanted signals.

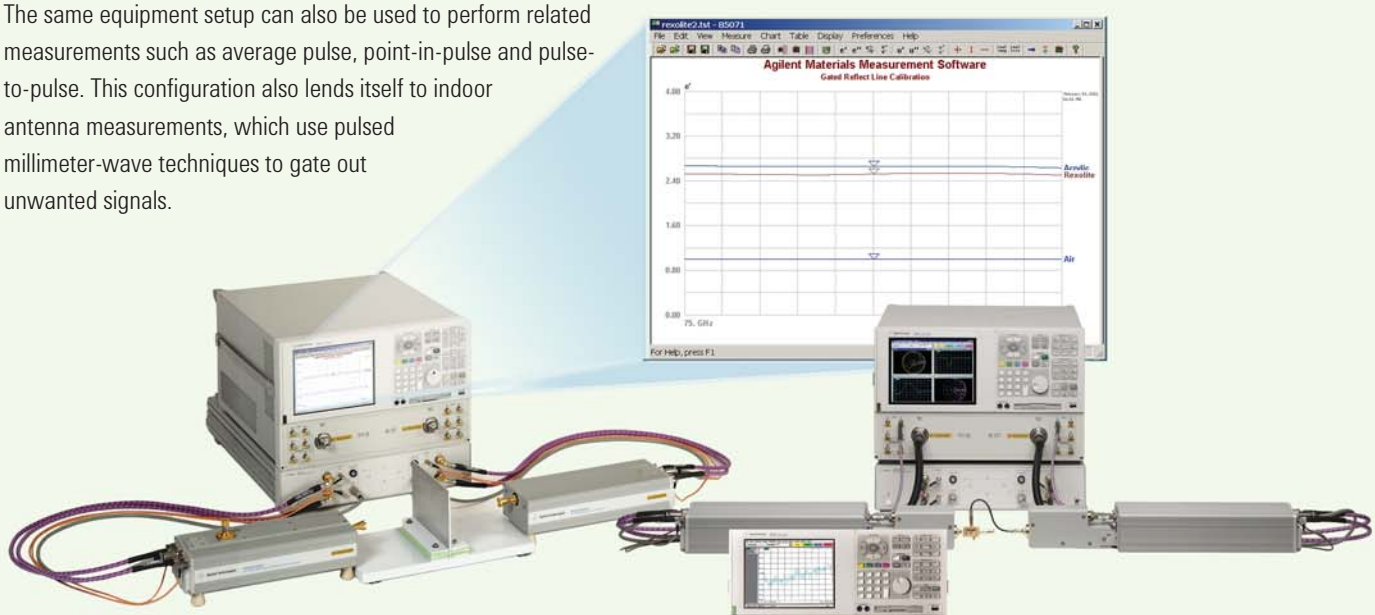


Figure 4. An intuitive software interface enhances materials measurements using the free-space calibration technique (Agilent 85071E).

Beyond on-wafer, pulsed and antenna applications, millimeter-wave solutions are also widely used for materials measurements. Figure 4 shows a W-band system, 75 to 110 GHz, performing materials measurements in free space. Due to the small size of the W-band waveguide interface, the free-space technique allows for a more manageable sample size (versus the minuscule size of the W-band waveguide interface). It also makes it possible to utilize Agilent's unique gated-reflect-line (GRL) calibration technique, which provides high accuracy without the addition of extra — and often expensive — hardware.

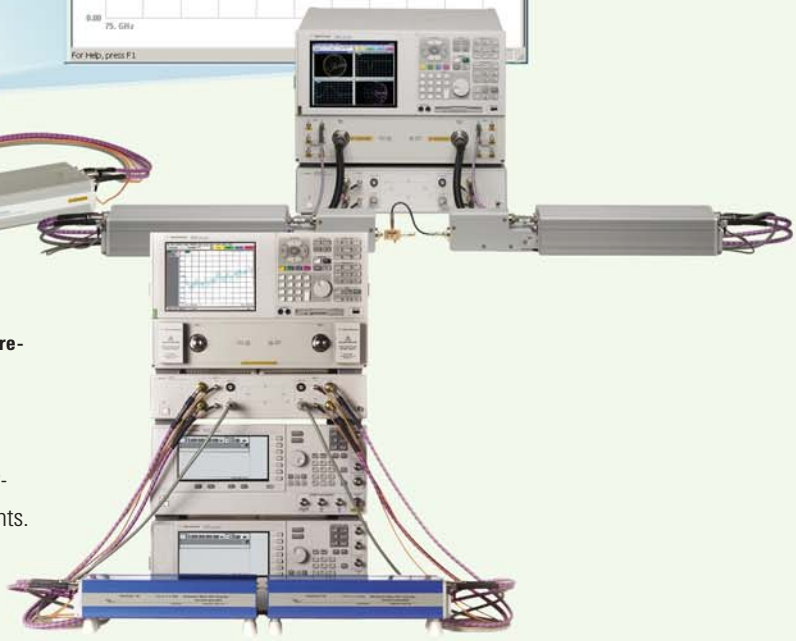
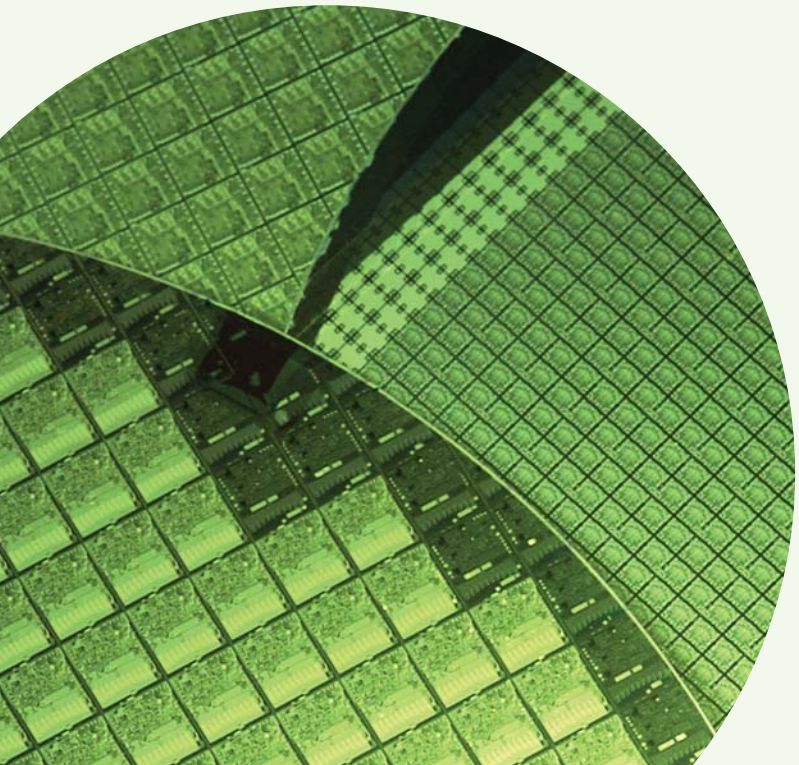


Figure 5. The PNA Series network analyzer is easily adapted to address a variety of millimeter-wave applications.



Conclusion

As shown in the preceding examples, the PNA Series network analyzer millimeter-wave solution can be adapted to meet the needs of several different applications (Figure 5). This type of versatile solution is often the most practical way to address today's broad range of applications and disciplines. It also reduces the need for multiple single-purpose measurement systems.

For future banded millimeter-wave applications, the Agilent PNA-X network analyzer (N5242A) also can address all of the measurements described here. To take advantage of the newly available functions and capabilities, simply substitute the N5242A for the PNA (E836xB) in each solution shown.

Enhancing Automotive Electronic Test with LXI

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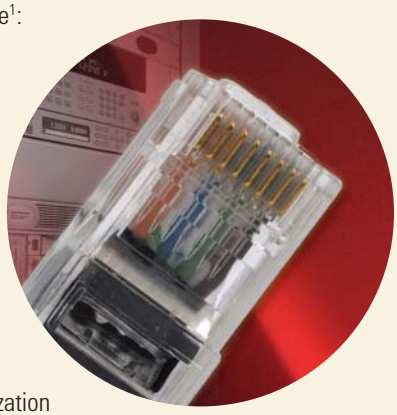
Figure 1. Agilent's LXI-compatible 34980A LXI multi-function switch/measure unit allows for insertion and removal of plug-in cards while power is on.

The automotive industry's highly competitive nature puts intense pressure on electronic manufacturers to boost quality while lowering costs. Activities such as electronic functional test are often viewed as necessary evils that must provide a high return on investment.

Enter LAN eXtensions for Instrumentation (LXI), an architecture for next-generation test systems based on proven, widely used standards such as Ethernet. Combined with the time-tested principles of providing just enough cooling, power, shielding and physical size to provide superb measurements in modular and traditional form factors, LXI's appeal is bolstered by its availability in bench-top instruments, providing excellent performance at competitive prices.

System designers who test automotive electronics can use LXI to maximize performance, minimize cost and plan for the future. There are at least nine good reasons to consider LXI for present and future test systems, as described in the April 2006 edition of *LXI ConneXion* magazine[1]:

1. Ease of use
2. Performance
3. Cost
4. Scalability
5. Longevity
6. Flexibility
7. Rack space
8. Distributed systems
9. IEEE-1588 synchronization



1. Ease of use

With the year-to-year changes in new car models, automotive electronics manufacturers must bring new products to market quickly. Rapid test system creation depends on getting instruments connected and systems running as soon as possible, which not only saves time but also enables manufacturers to focus on verifying the functionality of a module and its subassemblies.

Many of these systems are created with VXI- or PXI-based hardware and controlled with either an embedded PC or standalone PC connected through an interface card and cable. LXI solves four key problems developers would typically face under these methods:

- **Interface:** Rather than an MXI or GPIB interface, LXI uses Ethernet, eliminating the need to install an additional interface card in the PC. In addition, there are no proprietary cables or software.
- **PC configuration:** Because a PXI cardcage is an extension of the PC backplane, the whole system must be rebooted every time a card is inserted or removed. With LXI, PCs do not require rebooting when connecting or disconnecting instruments. What's more, some modular LXI instruments allow for "hot-docking" of cards while the power is on (Figure 1).

- **Drivers:** When a PXI system reboots, the PC uses an instrument discovery process to identify newly connected devices, which usually requires operators to download and install device drivers. The LXI standard specifies the use of IVI-COM drivers, making it easier to work in a variety of development environments. And some LXI instruments can be programmed directly through Standard Commands for Programmable Instruments (SCPI) when greater functionality or performance is required.
- **User interface:** With no front panel interface, using PC-based system software to diagnose problems in PXI and VXI devices can be difficult. With benchtop LXI instruments, the front panel interface makes it easy for developers to experiment with an instrument. While most modular LXI instruments lack a front panel, their built-in Web interface makes it possible to learn the capabilities by simply opening a Web browser on the connected PC. The browser function also makes it easier to see what's happening with the equipment, simplifying system support and ensuring greater uptime.

2. Performance

Automotive electronics testing includes everything from complex power train control modules requiring hundreds of tests, to simple airbag squib modules, to telematic/infotainment modules that may involve time-consuming transfers of huge data files. These tests often challenge GPIB's maximum data rate of roughly 1 MB/s. With LAN, I/O transfer speed is becoming a non-issue with 1-Gbit/s connections becoming commonplace and 10-Gbit/s on the way.[2]

I/O performance should not be an issue for LXI devices in typical automotive applications that require both transactional programming and transfers of large data blocks such as waveforms captured by digitizers. In transactional programming, there is a well-understood issue around LAN latency. Instrumentation vendors are reducing the number of required communication cycles by preloading instructions to LXI devices.

3. Cost

Minimizing the overall cost of test requires fast, reliable testing at as low a price as possible. Some trade publications have suggested that functional test adds no value: At this late stage, most manufacturers have inspected incoming parts, performed X-ray inspection and completed in-circuit test. While these steps do improve product quality, they do not eliminate the need for functional test because they cannot detect faults due to post-assembly product failures, design errors or inaccessible nodes.

Automakers' seemingly conflicting requirements compound matters. Instruments that deliver the necessary capabilities and performance at an attractive price can solve these issues, as can careful consideration of both initial hardware cost and recurring costs such as spares, warranties, local versus return-to-factory repair options and availability of rental equipment. In many cases, an instrument-by-instrument price comparison will show up to 40 percent reductions in the cost of LXI versus PXI hardware.[3]

It is also worthwhile to account for the learning-curve costs of cardcage instruments versus LXI. Cardcage instruments require the use of different software drivers for each development environment such as LabVIEW, Visual Basic and C++. LXI instruments generally offer a choice, enabling use of either drivers or SCPI.

4. Scalability

Figure 2 shows a typical automotive electronic functional test system built with LXI devices: expandable reed relay matrix, many armature-relay load switches, many channels of arbitrary waveform output and many channels of D/A conversion. In a cardcage-based system, these devices can quickly fill every slot, and the addition of just one more device requires another cardcage and computer interface. For systems requiring just a few cards, the cardcage adds cost and consumes space, though the empty slots allow for future expansion. LXI instruments provide the desired functionality, making it easy to upgrade functionality without adding a cardcage or computer interface. At most, the system may require the addition of a low-cost LAN switch to provide ports for added LXI devices.

Figure 2. In an automotive test system, LXI components enable greater scalability and flexibility to meet present and future needs.

5. Longevity

Figure 3 provides a comparison of various interfaces over the past 30-plus years. Most noteworthy is the continuous improvement in LAN performance while maintaining backward compatibility, suggesting that it will continue as a dominant force in the computer industry for a long time to come.

Extensions designed into the LXI Standard ensure that it will meet the foreseeable needs of the test and measurement industry, a critical requirement of the automotive electronics industry that supports an active aftermarket and long product lifetimes.

6. Flexibility

Cardcage-based solutions limit the optimal instrumentation placement in a test rack. For example, system creators will find it useful to put switching in one low-cost subsystem and stimulus/measurement instruments in another, simplifying service and avoiding use of high-cost, high-performance backplanes to control slow relays (often the case in PXI or VXI cardcages).

LXI instrumentation enables a better approach: A modular switch/measure unit equipped with an internal digital multimeter (DMM) and a selection of switching cards offers a low-cost method of creating a dedicated switching subsystem. The use of LAN also makes it possible to place the LXI-based subsystem farther from the host PC and closer to the unit under test.

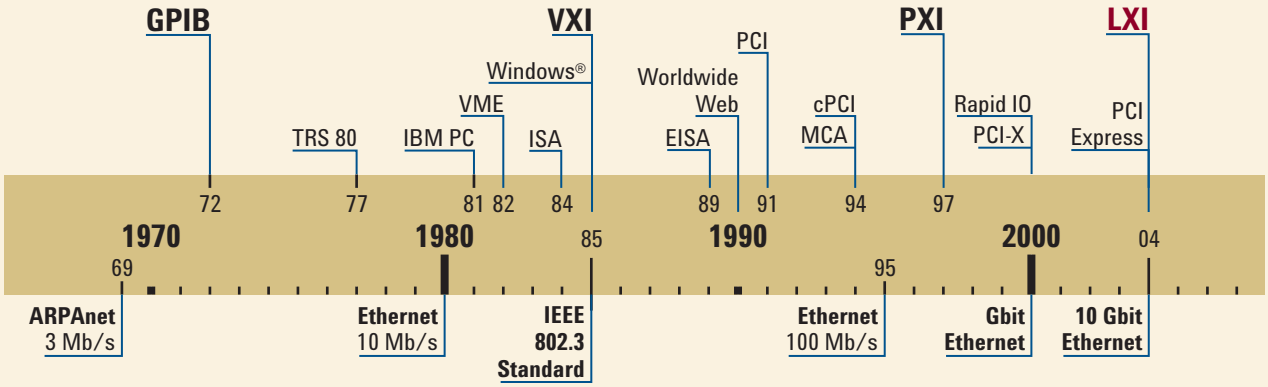


Figure 3. LAN has evolved — and maintained backward compatibility — while other interfaces have come and gone.

Few cardcage-based power supplies meet the current requirements of many automotive electronic modules and require external power supplies based on different architectures. Agilent has updated existing designs to be LXI compliant, housing them in compact, rack-friendly enclosures. Examples include the Agilent N5700 series of high-power supplies and the Agilent N6700 series of modular supplies (Figure 4).

Figure 4. Some LXI-compliant power supplies have size, power and functionality advantages over GPIB and PXI alternatives.

7. Rack space

An LXI-based functional test system could be assembled in a rack as small as 750 mm tall (Figure 5). This space efficiency is due in part to LXI-based devices such as an eight-slot switch/measure unit with a built-in DMM (second position in rack) and a 1U modular power system (lowest position in rack).

To achieve maximum density, system developers often use cardcage-based instrumentation. With VXI, a C-size cardcage can hold up to 12 high-performance instruments in about 6U, but this is often an expensive solution. PXI also provides high density, but its compact 4U size has four key shortcomings that are addressed by LXI:

Card size: Due to PXI card size, it may be necessary to use more than one slot to achieve the needed functionality. LXI instruments, on the other hand, can be created in a variety of sizes to ensure they fulfill their intended use.

Shielding: PXI cards are susceptible to interference. For example, a Signal Conditioning eXtensions for Instrumentation (SCXI) power supply that emits high levels of magnetic interference can lower the performance of an adjacent PXI DMM, potentially lowering DMM performance by a full digit of resolution. LXI devices are inherently shielded because they are fully self-contained.

Cooling and power: Cardcages must provide sufficient cooling and power supply capacity to handle a maximum number of instruments or relays at one time. In demanding systems, it may be necessary to upgrade to one or more higher-cost mainframes capable of providing the required cooling and power. Automotive electronics applications also often require instrumentation output voltages that exceed the voltage capability of many PXI mainframes. LXI instruments are generally designed to provide the required power, voltage and cooling for their target application.

Figure 5. With LXI, a functional test system can fit into a rack that is just 750 mm tall.

8. Distributed systems

Automotive production test systems typically co-locate all instruments. However, there is an inherent benefit to applications such as durability test systems, R&D test systems and production validation systems when operators can place LXI instruments where the measurement needs to be made.

Figure 6. LXI-based switching modules enable the creation of powerful remote test systems.

Production test systems also can benefit from a remote test-head. With off-the-shelf LXI switch modules, it is possible to create a test fixture that automatically adapts to any engine control module coming down the line, for example.

The ability to put the stimulus and measurement instruments where they are needed — with minimal or no cabling back to the core of the system — is a feature unique to LXI. Modules such as the Agilent L4400A series are designed for this type of remote or distributed application (Figure 6).

Another factor that favors LXI is remote debugging and trouble-shooting. Service technicians with remote access privileges can diagnose a test system from practically anywhere using a Web browser. If a LAN-connected webcam is added to the system, the remote technician can even see what is happening as they troubleshoot.

9. IEEE-1588 synchronization

In high-volume production lines, the ability to shave even one second of test time per module may be worth thousands of dollars. In such cases, any change to hardware or software that causes an increase in test execution time is unacceptable.

LXI addresses test time through extensive triggering capabilities, beginning with a standardized trigger bus in Class A LXI instruments. LXI also provides a new way to improve test execution time: self-triggered measurements based on a precise real-time clock are synchronized from instrument to instrument. With this capability, measurements can be performed without intervention from the host computer, minimizing or even eliminating trigger wiring in a test system and reducing I/O bottlenecks.[4]

Conclusion

LXI is built for the long haul and is well-suited to automotive electronic test. Its main benefits are in cost, scalability and ease-of-use, but LXI also offers advantages in performance, longevity, flexibility, synchronization and rack space. More information is available online at www.lxistandard.org and www.agilent.com/find/lxi.

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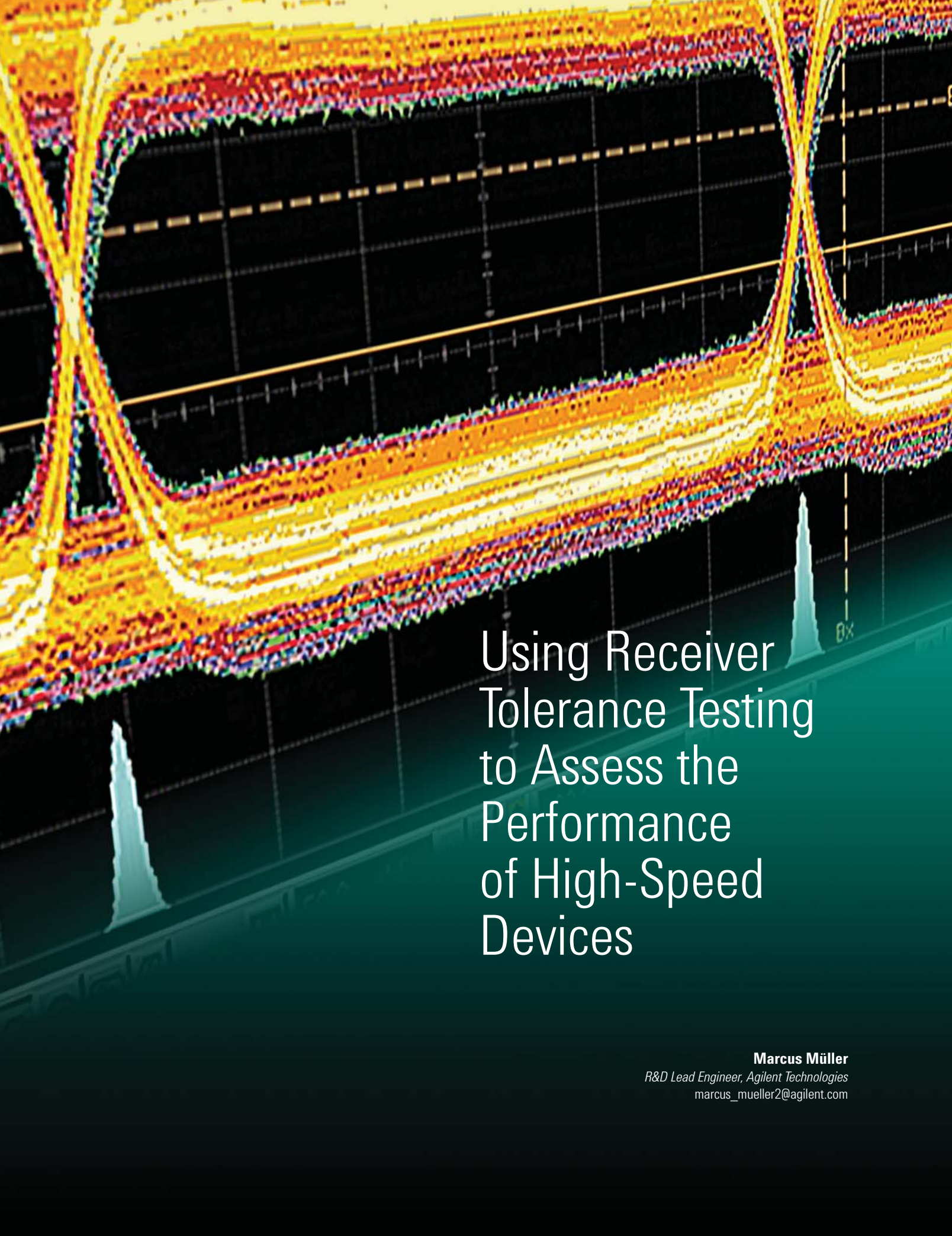

Using Receiver Tolerance Testing to Assess the Performance of High-Speed Devices

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The landscape of data communications and computing has undergone dramatic changes in the past five years. What used to be parallel-clocked or source-synchronous buses have been replaced by high-speed serial architectures with embedded clocks. Today, a typical PC contains a PCI Express graphics port (serial at 2.5 Gb/s, soon to be 5 Gb/s) instead of a parallel Advanced Graphics Port (AGP) and Serial ATA drives (at 1.5 or 3 Gb/s) instead of parallel IDE or SCSI — either of which were recently state-of-the-art technologies. The dominance of high-speed serial links, especially in the cost-sensitive PC market, was made possible by incredible advances in transmitter and (especially) receiver technologies: clock-data recovery, clever coding schemes, receiver equalization and transmitter pre-emphasis have been major factors.

As receivers become more complex, thorough testing becomes more difficult. Until recently, typical receiver-tolerance test systems included numerous pieces of equipment. These systems were expensive, bulky, difficult to set up, tough to control and extremely hard to calibrate. Today, the necessary functionality is available in standalone bench instruments such as the Agilent J-BERT N4903A high-performance serial bit error ratio tester (BERT). This instrument can perform full receiver characterization over a wide range of parameters, in addition to other critical measurements such as bit error ratio (BER) and jitter.

Basics of receiver tolerance testing

The basic point of receiver tolerance testing is to assess how well the device under test (DUT) can handle bad signals. There are two important aspects to this: the definition of a "bad" signal and the parameters that define expected operation of the DUT.

A receiver tolerance setup tests multiple features of the receiver: clock recovery from the data stream, jitter tolerance, noise immunity and the ability to compensate for the effects of band-limited transmission channels. Receiver tolerance testing is often termed "jitter tolerance" testing because measurements are jitter related; however, noise immunity in particular is typically included. Additional aspects of receiver testing include operation with low signal levels, at signal offsets and with stress-data patterns. The actual worst-case bad signal depends on the application, which is usually defined in the relevant standard.

It is often difficult to determine if the device works with a given signal. In transmitter measurements, we attach a test instrument such as an oscilloscope to its output and directly measure the parameter of interest. In contrast, receiver testing relies on indirect observations. The only method that comes close to a direct measurement of receiver performance is a BER measurement: The data stream at the output of the receiver is compared to expected data and the BER is calculated by dividing the total number of compared bits into the number of error bits. This depends on access to the device output, which cannot be taken as a given.

Test setup and device types

On a high level, the general setup for receiver-tolerance testing is fairly straightforward (Figure 1). A pattern generator creates a digital data signal with a certain amount of jitter, noise or other impairments and sends it to the DUT. However, determining the device's ability to tolerate the input signal requires access to the data after it is received by the DUT.

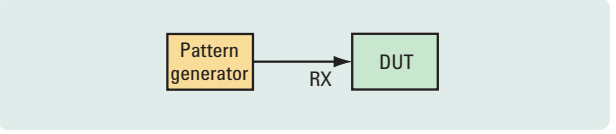

Figure 1. High-level setup for a receiver tolerance test

Typical high-speed serial integrated circuits are serializing/de-serializing transceivers, integrating both a transmitter and receiver in a single device. In this case, it is possible to use the device's transmit output to resend the received data and then measure the BER with an external error detector. In most cases, the loopback is done within the chip; however, the received data can also be looped externally on a test adapter or test board.

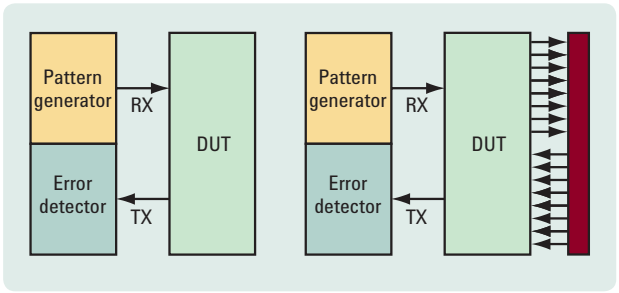

Figure 2. Internal (left) and external (right) loop-back setups for receiver tolerance test of serial high speed transceivers

Measurement procedure

Whether the receiver works or not is seldom a yes/no decision: A receiver may be able to handle the bad test signal most of the time, but may occasionally cause bit errors. If the device output is available, the BER can be used to establish a good/bad threshold. Most standards specify a limit for the acceptable error ratio, often at 10^{-12} but sometimes even lower. Unfortunately, proving that the device operates at 10^{-12} or lower requires at least $3x10^{12}$ error-free bit compares. Even at high data rates, this takes a long time (e.g., more than five minutes at 10 Gb/s). If the error ratio is high, the measurement can be terminated after detecting just a few errors, reducing the time spent on a bad device.

Verification of receiver compliance with a standard begins with knowledge of the required test signal components from the specification. Compliance testing requires application of the specified signal impairments at the receiver input, measurement of BER and a comparison of the results with the specified BER limit. In many cases, though, a single test is not enough and it is necessary to test different combinations of jitter and noise components, sometimes at different signal levels. In fact, almost every standard specifies the amount of sinusoidal jitter the device must tolerate as a function of the jitter frequency; the lower the frequency, the more jitter must be tracked. This procedure tests the clock data recovery circuit of the receiver. Figure 3 shows an example: The solid black line is the standard mask, the dots show each measurement point and the color of the dots indicates the BER at each point (green if the BER is lower than 10^{-12} and red otherwise). Since all points are green, the example device passed the test.

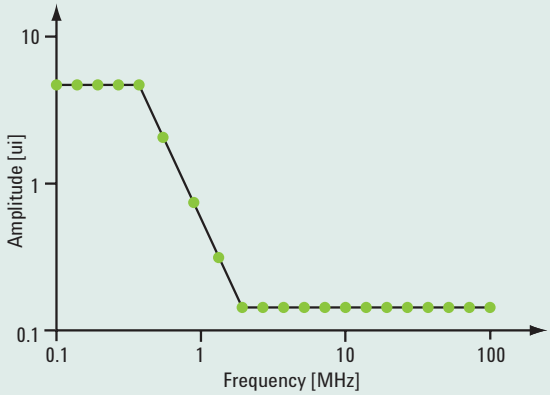

Figure 3. Compliance test with a sinusoidal jitter tolerance mask. Green dots show measured points that passed a BER test at 10^{-12}.

While a compliance test results in a pass/fail decision and is therefore used mostly in production environments, it is also useful to know how well the device works. Such a characterization typically sweeps a parameter such as sinusoidal jitter frequency as in the preceding example. However, instead of just checking the receiver's ability to tolerate a given level of sinusoidal jitter at the current frequency, the goal is to quantify exactly how much jitter it can tolerate. This is done by increasing the jitter level step by step until the device fails, as shown in Figure 4. Receiver characterization is not limited to sinusoidal jitter: BER can also be measured as a function of inter-symbol interference, random jitter or any other variable the test setup can control.

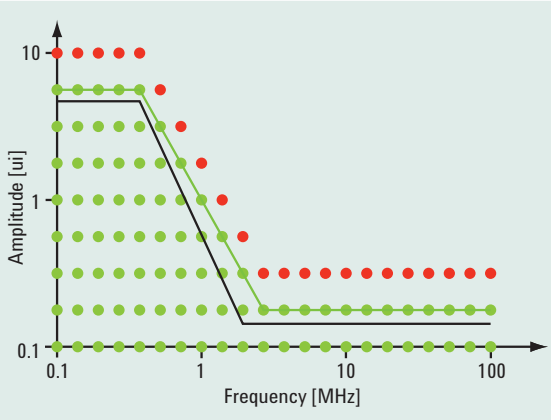

Figure 4. Characterization measurement with sinusoidal jitter. Green dots show measured points that passed; red dots measured points that failed a BER test at 10^{-12}.

Test signal generation

So far, our discussion has assumed the ability to create test signals with various kinds of jitter and other impairments. It is now time to examine how these signals are generated and thereby gain a better understanding of the test instrumentation.

Random and periodic jitter generation

The most important part of the signal generation for receiver tolerance testing is non-correlated jitter: random jitter and deterministic period jitter. The two main methods for jitter generation are phase/frequency and delay modulation. For historical reasons dating back the first SONET standard, typical tests often use periodic jitter with a sinusoidal waveform; such signals seldom occur with real devices, but they allow for easy testing of CDR/PLL performance versus jitter frequency.

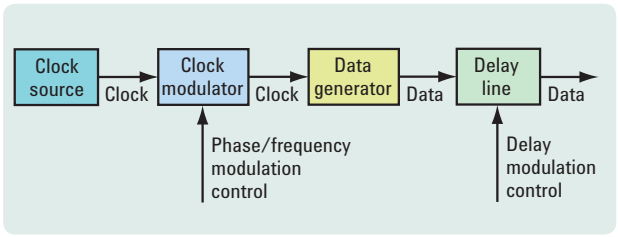

Figure 5. Clock and delay modulation in the pattern generator

Phase/frequency modulation, which is typically located in the clock synthesizer section of the pattern generator, consists of the clock modulator itself (e.g., an I/Q modulator) and control-signal generation (Figure 5). Due to bandwidth limitations in the modulator, the choices of modulation frequency and modulation amplitude are limited; the maximum jitter amplitude depends on the frequency, as illustrated by the blue line in Figure 6. At low frequencies, it is possible to achieve very high modulation of several hundred unit intervals (UI). Clock modulation is used mainly for lower speed sinusoidal jitter, utilized in clock data recovery testing.

The delay modulator is located in the data path of the instrument and consists of a control-signal generator and a voltage-controlled delay line (Figure 5). Typical delay lines have a maximum modulation amplitude of several hundred picoseconds, independent of the modulation frequency (black line in Figure 6). Because the delay time is constant, the maximum modulation in UI depends on the data rate. The main advantage of voltage-controlled delay lines is an extremely high modulation bandwidth, which makes them the method of choice for higher speed period and wideband random-jitter generation.

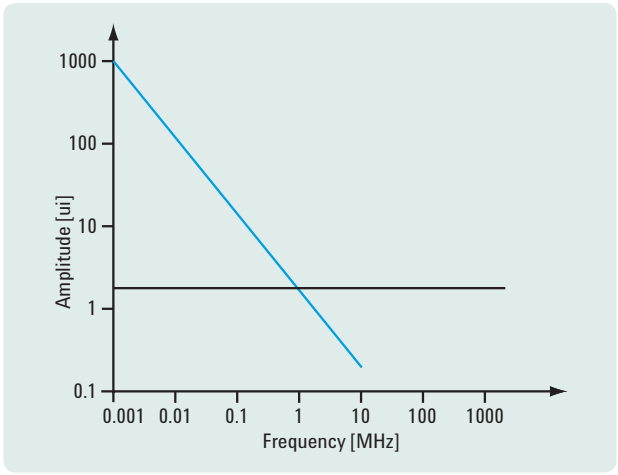

Figure 6. Maximum sinusoidal jitter amplitude, as a function of jitter frequency. Blue line: frequency/phase modulation; Black line: delay modulation.

Voltage control of the delay makes it very easy to use an arbitrary waveform generator to create jitter distributions with arbitrary time waveforms and probability distributions. This enabled the OIF/CEI standard to specify a very special jitter tolerance signal, bounded uncorrelated jitter (BUJ). Generated from a heavily filtered pseudo-random binary sequence (PRBS), it emulates crosstalk and other bounded Gaussian effects.

Inter-symbol interference

Today, most high-speed serial receivers feature some type of equalization to compensate for inter-symbol interference (ISI), the effect of a band-limited channel. Testing these equalizers requires a signal with a certain amount of ISI. The method of choice uses a real trace on a lossy board material, which has a more realistic loss characteristic than a simple RF low-pass filter. Several standards (e.g., XAUI) have specified compliance backplanes, which are commercially available (Figure 7). For custom designs, it may be necessary to develop an application-specific ISI test board.

Figure 7. Tolerance test setup for inter-symbol interference using an external compliance backplane

The disadvantage of external board traces is that they need to be inserted manually into the signal path. If we want to make measurements over different trace lengths, or make comparisons with and without ISI, automated measurements are almost impossible, or require numerous expensive and bulky microwave-grade relays. One solution is to build a special test board that has several traces in binary increments (e.g., 1", 2", 4", 8", 16", 32"), connecting the traces via relays such that each one can be switched into the signal path, making it possible to create every trace length between 1" and 63" (Figure 8). Of course, the relays may cause the results to differ from a real backplane; however, with the fine trace-length granularity, it will almost always be possible to find a trace that is close enough.

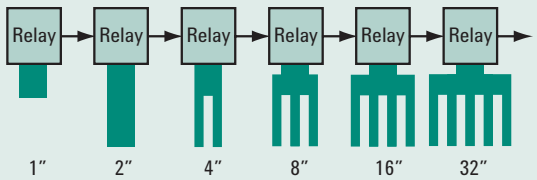

Figure 8. ISI generation using a backplane with switchable traces

Level interference

The last major signal impairment is level noise, which is added to the test-data signal through passive adders (Figure 9). The modulation control signal is usually a sinusoid at frequencies ranging from several hundred megahertz to several gigahertz. Level interference testing comes in two variants: common mode and differential mode. Common mode uses the same signal on both signal rails and tests the common mode rejection of the receiver. In differential mode, the two control signals have a 180-degree phase offset, which tests the receiver's ability to work with small differential amplitudes. Level interference is usually applied after the compliance channel or at the near-end, as seen from the device (refer back to Figure 7).

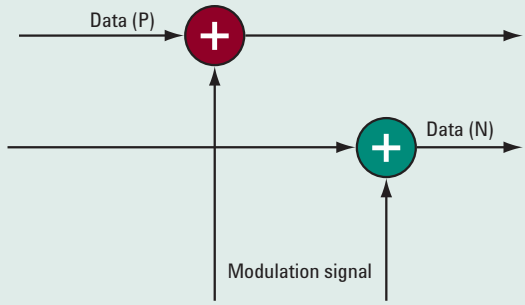

Figure 9. Level interference circuit using passive adders

Calibration

Calibration may be the most challenging aspect of receiver tolerance testing. While is it fairly easy to create a very bad signal, it is difficult to create a signal with precise amounts of jitter, inter-symbol interference and level noise. Without a good calibration strategy, measurements will not be reproducible, making the results essentially meaningless.

Calibration of ISI and level interference is fairly straightforward: Channel S-parameters can be measured directly with a network analyzer and level noise is easily measured on an oscilloscope. Unfortunately, many jitter measurement instruments have tremendous difficulty calibrating the jitter components of the receiver test signal. The first issue is the ability to measure large jitter amplitudes. Most jitter measurement methods are limited to about 0.5 UI total jitter, peak-to-peak, which is sufficient for real-world signals. As shown above, however, a jitter tolerance setup can create several hundred UI of total jitter. The second issue comes from the artificial nature of test-signal jitter. In a sense this violates the valid real-world assumptions measurement instruments must make in order to separate jitter into its components. For example, a common assumption is that spectrally wide components are random jitter, which is not necessarily the case for complicated period jitter waveforms.

To date, the best strategy for jitter calibration is to use special test equipment for each jitter component and measure them one by one. Low-frequency sinusoidal jitter can be measured with a special spectral technique, Bessel Nulls; this works even at extremely high modulation amplitudes. Random jitter and higher speed period jitter are measured with an oscilloscope within the range of the instrument; outside of the range, the delay control signal can be measured directly. The drawback to the "divide and conquer" approach to calibration is the assumption that the individual components are independent and add via convolution; however, in practice this assumption continues to remain valid.

Conclusion

It seems likely that the dramatic pace of evolution in data communications and computing will continue unabated. The ability to test ever-faster serial architectures — and their receiver devices — depends on measurement tools that provide meaningful measurements of critical parameters such as jitter and BER. In both R&D and manufacturing, receiver tolerance is perhaps the most challenging measurement task in high-speed serial device characterization. This task is made easier with standalone bench instruments such as the Agilent J-BERT N4903A high-performance serial bit error ratio tester. Introduced in 2006, the N4903A was the first commercially available instrument to include sources for testing of all jitter components (Figure 10).

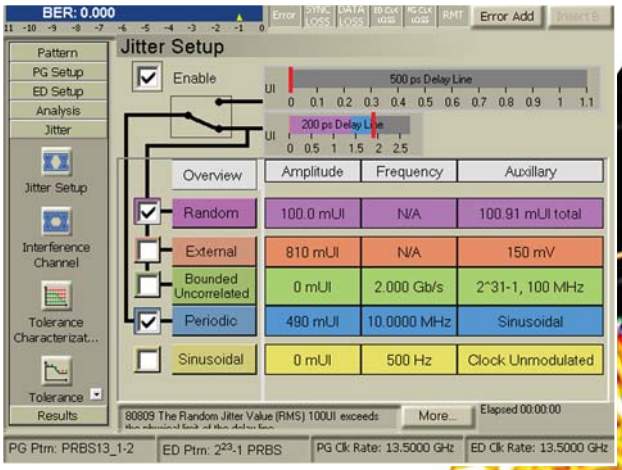

Figure 10. Example of the N4903A user interface showing the manual jitter set-up page

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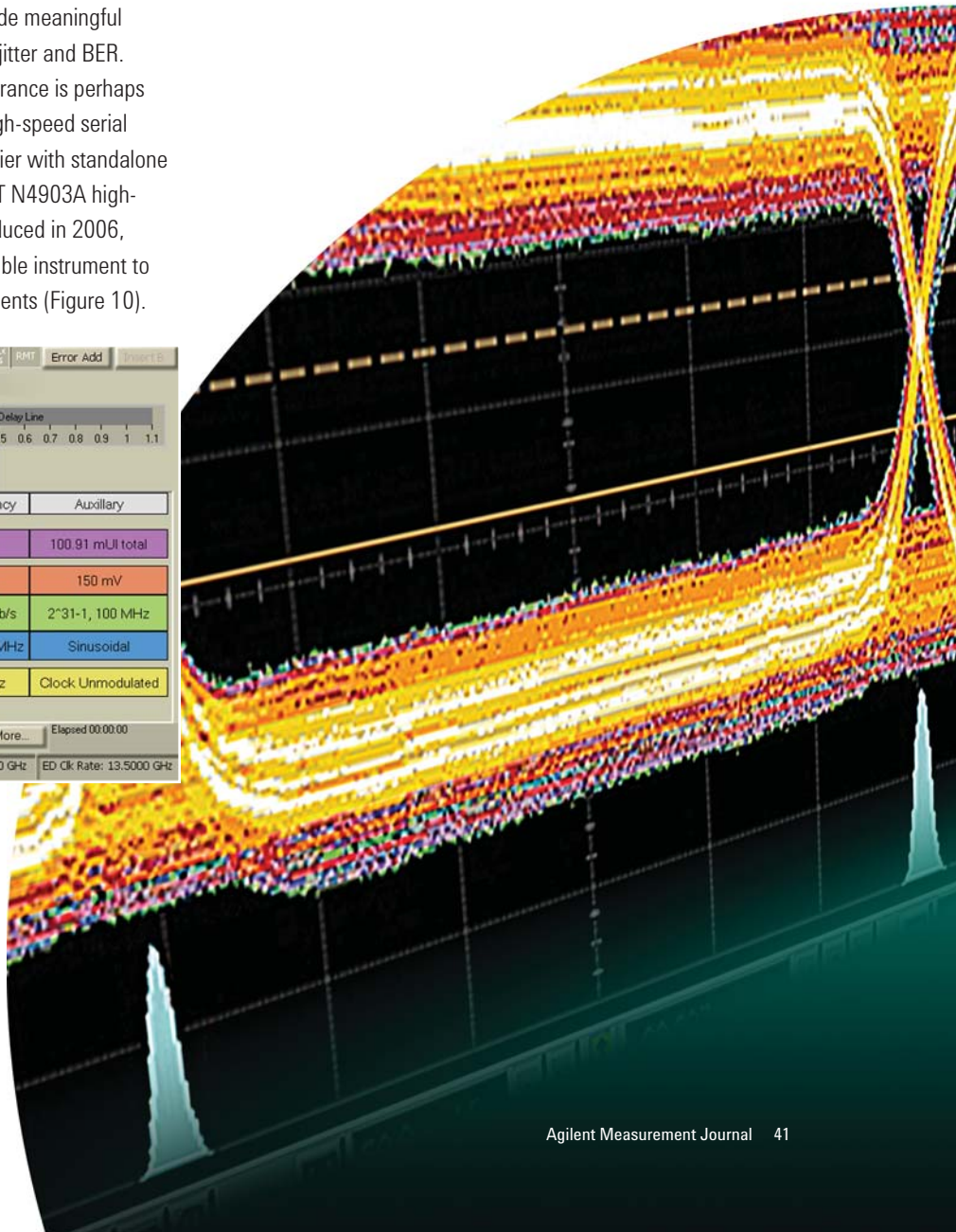

Using MicroBlaze Trace Core to Accelerate Debug in Xilinx Embedded Designs

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For engineers working on embedded designs, advances in measurement-core technology are greatly enhancing their ability to trace microprocessor activity inside field-programmable gate arrays (FPGAs). Specifically, the second-generation Agilent Trace Core (ATC2) works hand-in-hand with Agilent logic analyzers and has been customized to capture signals from Xilinx MicroBlaze embedded processors. This customized trace core is called the MicroBlaze Trace Core (MTC) in this application.

In the past, caching and pipelining made it difficult to trace embedded-processor activity on the external memory bus. Today, the ability to probe directly behind the cache makes it easy to observe every execution step. This also simplifies time correlation to events external to the FPGA, increasing the efficiency of system debugging and validation. As an example, we will describe how the Agilent MicroBlaze Trace Toolkit enables the validation of a basic MicroBlaze application that includes an interface to external double-data-rate (DDR) memory.

Outlining the basic test philosophy

The example system incorporates a significant portion of its design within a Xilinx Virtex-4 FPGA and includes a memory controller for the external DDR memory (Figure 1). The ability to track system operation requires observation of MicroBlaze program execution and its interaction with external memory. As a starting point, it is often useful to check the memory interface by writing something simple, known and predictable — perhaps a counter — into memory and then reading back a few data bits. It is possible to check basic functionality by looking inside the FPGA while also observing timing external to the FPGA, either at a specific location for memory writes or at the FPGA pins for a memory read.

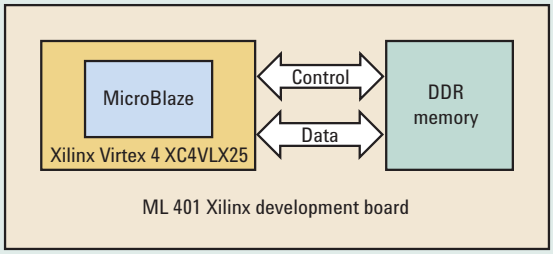


Figure 1. Digital system-under-test with external DDR memory

Combining MTC with logic analysis

Using the MTC in conjunction with an Agilent 16800 portable logic analyzer or 16900 series modular logic analyzer enables viewing of MicroBlaze activity inside the FPGA (Figure 2).

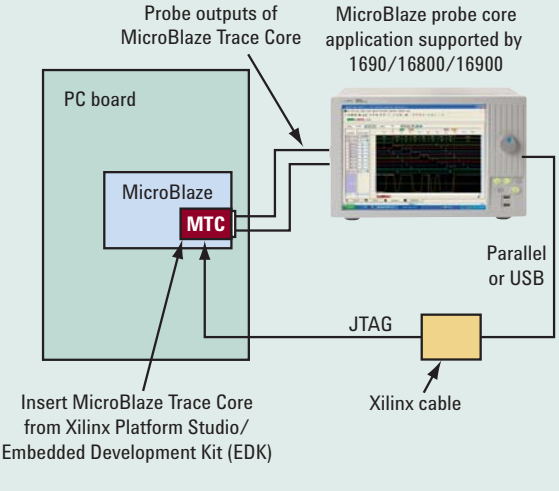


Figure 2. Block diagram of MicroBlaze trace solution

A Xilinx application available in the Embedded Development Kit (EDK) provides a mechanism for inserting the measurement core and a graphical user interface for defining its capabilities. When configuring the core, there is a tradeoff between the level of visibility and the number of FPGA pins required so it is important to consider what must be accomplished with the intended measurements versus the available pin resources. For example, signals such as the 32-bit program counter (PC) may have static upper significant bits so only the dynamic bits must be accessed. If only the lowest 10 bits of the PC are active, probing just six physical FPGA pins will enable viewing of program execution within the processor. (Selecting the Agilent Trace Core time-division multiplexing (TDM) option will halve the required pin count.) If none of the upper PC bits are static, then it is necessary to probe 17 FPGA pins. With additional pins it is also possible to view the data address bus and data values for memory reads and writes. Defining the core is done through the interface shown in Figure 3.

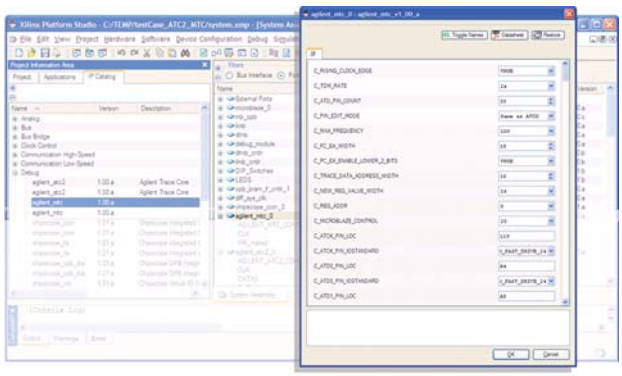


Figure 3. MicroBlaze measurement core definition in Xilinx Platform Studio

Defining resources for the MTC

The other tradeoff to consider is the number of resources required to implement the MTC as a function of visibility level. Fortunately, all acquisition occurs into the deep memory of an external logic analyzer so no FPGA Block RAM is required for such measurements. When only simple program execution is required, a core can be created that consumes only 218 lookup tables (LUTs) and 378 flip flops (Flops). Table 1 shows several other conditions that trade off resource consumption with the number of signals that can be seen.

Connecting to the target system

The choice of connection to the target system determines the level of internal MicroBlaze visibility and external DDR memory visibility. Many options exist for MicroBlaze devices: an on-board header with 0.1-inch spaced pins and flying lead probes, a Mictor connector, a Samtec connector or a SoftTouch footprint. The choice depends on personal preference but is often informed by the tradeoffs between the cost of board implementation, the cost of logic analyzer probe adapters and space available on the board.

Table 1. Resources required for MTC in several scenarios

Signals accessed	Inverse assembler output	Without TDM	With TDM
PC	Program trace (instruction addresses and mnemonics)	34 pins 207 LUTs 385 FFs	17 pins 218 LUTs 378 FFs
PC and data address	Data addresses for memory reads/writes, read/write indication	69 pins 320 LUTs 632 FFs	35 pins 354 LUTs 700 FFs
PC, data address and data	Data values for memory reads/writes. Data values and register numbers for register writes.	105 pins 436 LUTs 820 FFs	53 pins 497 LUTs 938 FFs
Minimal PC (10 bits + VALID_ INSTR + CLK)	Program trace (instruction addresses and mnemonics)	12 pins 138 LUTs 217 FFs	6 pins 144 LUTs 229 FFs

A direct connection provides the best performance when accessing external DDR memory. This can be done by soldering small wires to the DDR memory pins and then attaching logic analyzer flying leads to the wires (Figure 4). For ball grid array (BGA) packages, a BGA probe is often the best connection option (Figure 5). This approach ensures easy access to many signals while maintaining very high signal integrity.

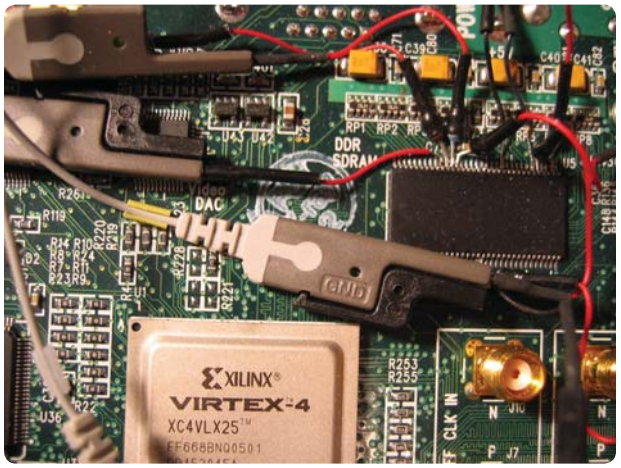


Figure 4. Physical connection to target system

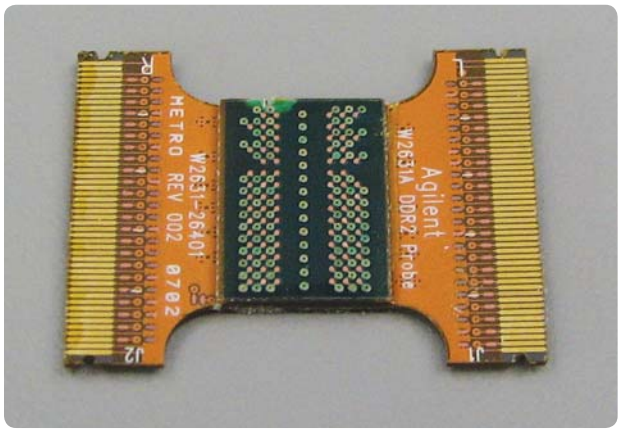


Figure 5. DDR BGA probe

Enhancing the tracing process

To automate the MicroBlaze trace process, Agilent and Xilinx co-developed the MicroBlaze Trace Toolset (Agilent E9524A). The toolset consists of a software application called the FPGA Dynamic Probe and a license that enables the application to recognize and work with the MTC. It also includes a MicroBlaze inverse-assembler tool.

The FPGA Dynamic Probe provides five main capabilities that make MicroBlaze capture a turnkey process:

- Make a Joint Test Action Group (JTAG) connection to the target
- Download the design files to one or more FPGAs
- Import bus and signal names associated with the measurement core
- Automatically map physical FPGA debug pins to logic analyzer channel inputs
- Automatically set up logic analyzer acquisition mode and thresholds

The basic FPGA Dynamic Probe interface shown in Figure 6 includes buttons that guide the user through these basic steps. The steps may be simple, but they automatically set up the logic analyzer with a variety of buses and signals to reveal program execution and provide access to the data bus (Figure 7). This process would require a significant amount of manual work without the FPGA Dynamic Probe application.

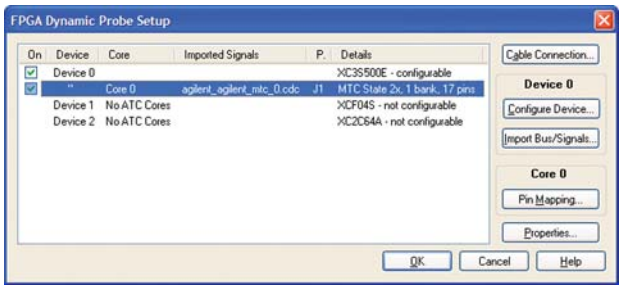


Figure 6. FPGA Dynamic Probe interface and setup steps

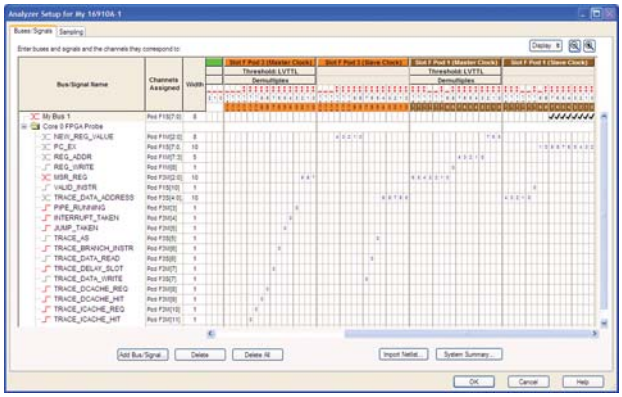


Figure 7. Automatic bus and channel setup on logic analyzer

In this example, automatic FPGA pin mapping found the 20 pins used for debug and determined which logic analyzer channels were connected to each FPGA pin (Figure 8). Normally, this would require a careful review of the schematics to identify the physical connection via PC-board traces from the FPGA to a suitable connector as well as the subsequent connections into the logic analyzer input channels. With the software application, this process takes just a few seconds.

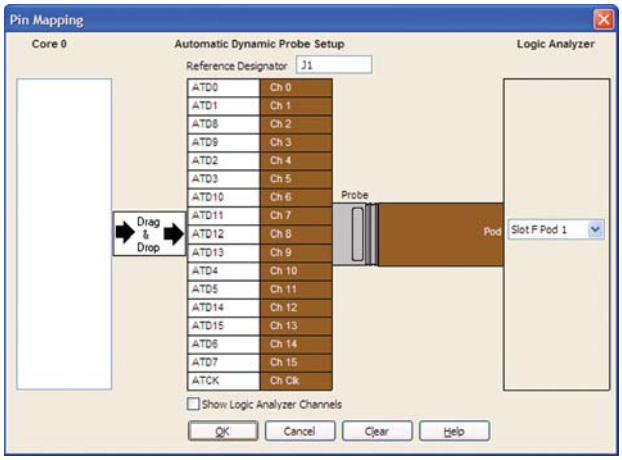


Figure 8. Automatic FPGA physical pin mapping to logic analyzer channels

Performing inverse assembly

Getting valid signals into the logic analyzer with appropriate bus and signal names is the first step toward revealing how the processor is executing commands. The next step is performing an inverse assembly to convert raw signal activity into MicroBlaze language. Adding the inverse-assembler tool within the logic analyzer is simple: first select the **Overview** tab at the bottom of the screen and then click **Tools>New Inverse Assembly>Xilinx MicroBlaze 5 Inverse Assembler** (Figure 9). The inverse-assembly tool is inserted after the acquisition module block and a properties tab allows entry of **Data Start Address** and **Program Start Address**.

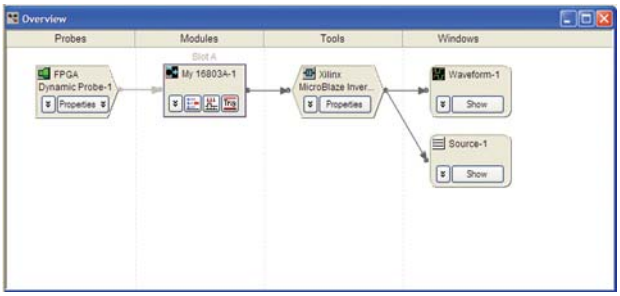


Figure 9. View in Overview window of added inverse assembler

The final step in the setup is performed through the **Listing** window by right-clicking on the address header field and then navigating to the directory containing the executable .elf file. This file is created after the program source code is compiled for the MicroBlaze processor; it is used to place the compiled program in memory so it can be run on the MicroBlaze processor. Pressing **Run** on the logic analyzer initiates a trace capture (Figure 10). In this example, the MicroBlaze executes commands that implement a memory controller performing writes to and reads from external memory.

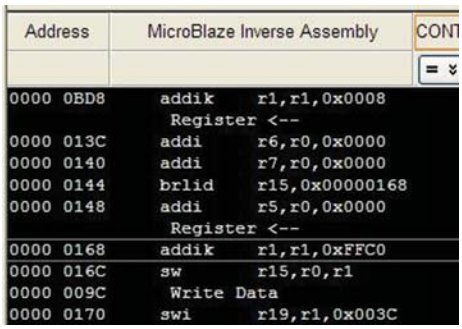


Figure 10. Inverse-assembly view

Correlating trace and source code

During hardware/software integration, it is often necessary to isolate hardware problems, software problems and improper interaction between the two. This type of troubleshooting is more effective with a view that correlates the inverse-assembled trace and the source code that produced it. The Agilent inverse assembler includes a source correlation tool that needs just the locations of the source code and .elf files to create a correlated view of both source and assembly (Figure 11).

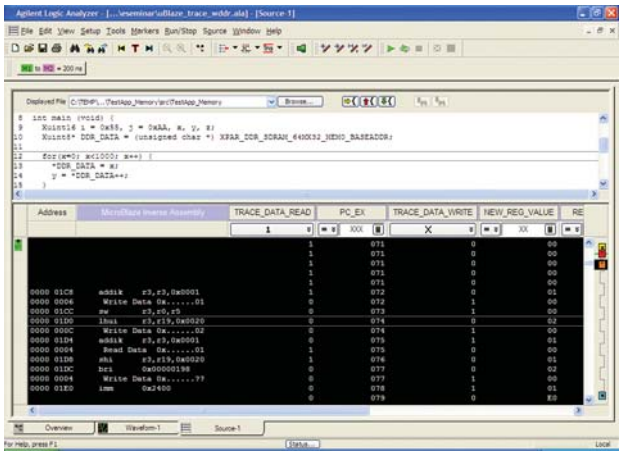


Figure 11. Correlated view of inverse assembly and source

Correlating external memory operations

A few simple steps expand the correlated view to include the hardware connection to external memory. The logic analyzer is first "split" into two analyzers, each of which connects to a different clock domain. The first connects to the MicroBlaze clock and the second to the DDR clock. With DDR memory, additional logic analyzer setup steps are required to define key DDR hardware signals such as RAS, CAS, Write Enable, Chip Select, the DQ strobe, CK and some data bits. Logic analyzer labels are defined with these signal names and logic analyzer channels are assigned to each label. These labels provide visibility into external memory data and also help qualify logic analyzer capture-and-search operations based on specific conditions such as a memory write.

The RAS, CAS and Write Enable signals form a word that defines the type of memory cycle (Table 2). It is easy to set up the logic analyzer to search through acquired data until it finds a captured memory cycle of interest.

Table 2. Memory cycles

Signal no.	Function	RAS	CAS	WE
1	Load mode register	L	L	L
2	Auto refresh	L	L	H
3	Precharge	L	H	L
4	Select bank activate row	L	H	H
5	Write command	H	L	L
6	Read command	H	L	H

A memory write operation provides a useful example. The inverse-assembly view shows when a memory write request occurs; a search forward through the captured trace for "command equals hexadecimal 04" finds the time when the memory write occurs. Placing a time-correlated tracking marker at that point and opening the Waveform Viewer around the marker reveals the timing of signals on the memory interface for the memory write (Figure 12). If the timing is correct, data is stable at the rising edge of the DQS and CK signals. The same process is used to check a memory read but the search string would be "command equals hexadecimal 05."

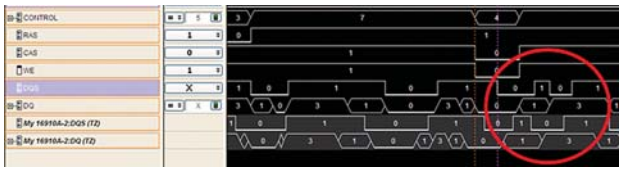
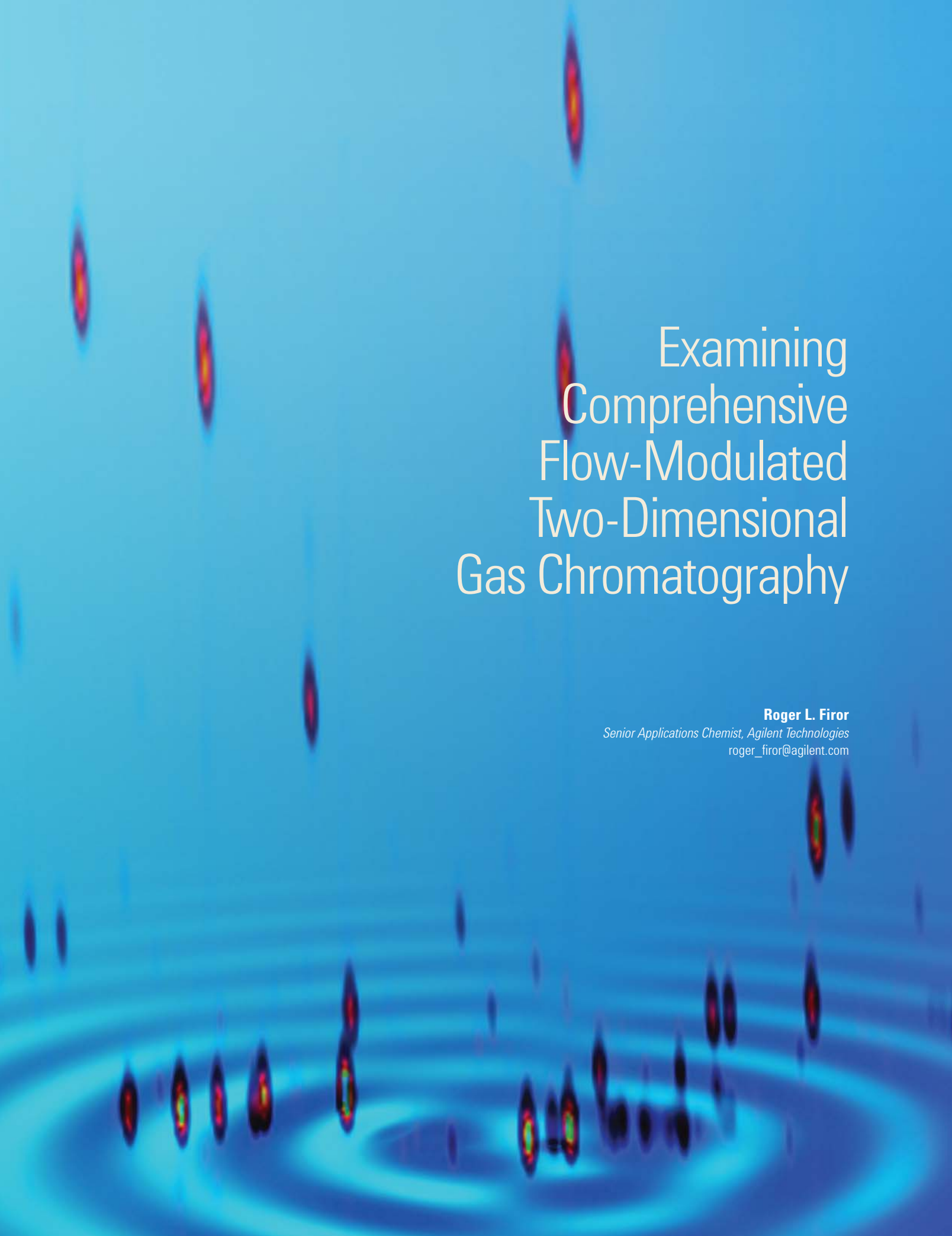


Figure 12. Capture of memory write timing

Conclusion

Tracking program execution while capturing hardware signals between an FPGA and external memory is faster and easier with MicroBlaze-focused measurement cores and logic analyzers that can be split for viewing of multiple clock domains. Even when the processor cache is on, the ability to probe behind the cache and view executed commands makes it possible to achieve good time correlation between inverse-assembly and external-memory trace. Automating these measurements puts essential validation and debug signals on-screen more quickly. Simplifying the overall process makes these powerful measurements more practical — and this saves time in the validation process and accelerates time-to-market for the final product.



Examining Comprehensive Flow-Modulated Two-Dimensional Gas Chromatography

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Gas chromatography (GC) is the most widely used tool in separation science today. It is so well established, however, many practitioners view it as a mature technology that offers little opportunity for innovation. Rather, its widespread use means any worthwhile innovation in hardware, software, or applications can have a significant impact. As proof, at least three significant developments have advanced the art of GC:

- Fast, high-resolution capillary columns have replaced packed columns of limited separation ability.
- "Hyphenated" techniques that couple gas chromatographs with mass spectrometers (GC/MS), for example.
- Electronic controls that provide very precise and repeatable control of flow and pressure in chromatographic systems.

One relatively recent development that has enhanced GC is two-dimensional GC, called "GCxGC" or "2D GC." This hyphenated technique is recognized for its powerful separation capabilities in the analysis of complex mixtures such as those found in the petrochemical and fragrance industries.

The 2D GC methodology utilizes two capillary columns of usually very different polarities installed in series. Between the two columns resides a device known simply as a flow modulator that is interfaced to an auxiliary programmable control module (PCM) on the GC through a three-way solenoid valve.[1] Within the flow modulator, analyte bands from the first column are collected in a fixed-volume channel and successively launched quickly into the short second column in very narrow bands (Figure 1). Any separation that occurs on the first column is preserved during transfer to the second column.

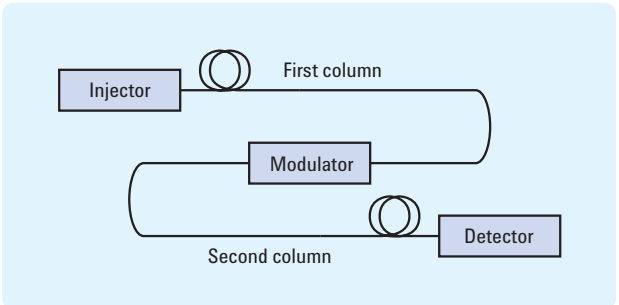


Figure 1. 2D GC utilizes a primary column (conventional separation), a flow modulator, a second column (very fast separation) and a fast detector.

Compared to one-dimensional separations, 2D GC can increase peak resolution and peak capacity, resulting in a greater number of individual compounds being separated. Per unit of time, its peak-generating ability is much greater than that of a single-column separation.

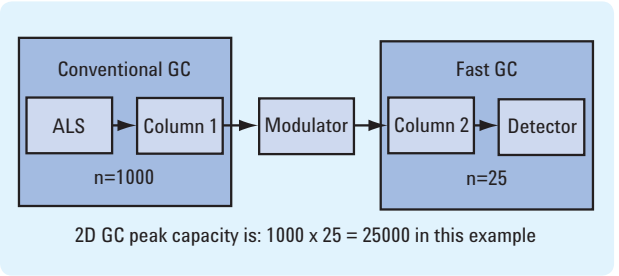


Figure 2. 2D GC provides a significant increase in separation power compared to 1D methods.

Creating a better modulator

The key component in a 2D GC system is the modulator. This device must transfer effluent from the first column to the second precisely and with high repeatability under a wide range of carrier flow rates and temperatures — without adding any extraneous chromatographic artifacts.

Most systems available today employ thermal modulation techniques in which rapid cooling (using a cryogenic jet) followed by rapid heating (using a hot-gas jet) immobilizes and then remobilizes the analytes. In such systems the cryogenic jet is always on and repetitive firing of the hot jet sends sharp bands of material to the second column for separation and detection.

The fabrication of conventional devices involves machining of stainless steel blocks. While this works well for simple devices such as unions, the complex structures required for controlled flow diversion (e.g., Deans switches or three-way splitters) are much more challenging. The need for low dead volume requires holes typically drilled at 0.25 mm inside diameter (ID) in size. This level of precision is possible only for short distances, making manifold construction very difficult and costly. The approach also results in significant thermal mass, which is undesirable in a chromatographic oven.

1. This concept was first demonstrated by John Seeley of Oakland University, Rochester, Michigan.

Agilent has developed a unique modulator that is simpler to operate and provides a lower cost of ownership compared to thermal modulation. Rather than using cryogenics, flow differentials trap or focus analytes as they exit the first column. This approach is based on Agilent's capillary flow technology hardware, which utilizes a new way of fabricating complex structures. Combined with several other improvements, this allows construction of in-oven devices that make difficult GC application problems easier to solve.

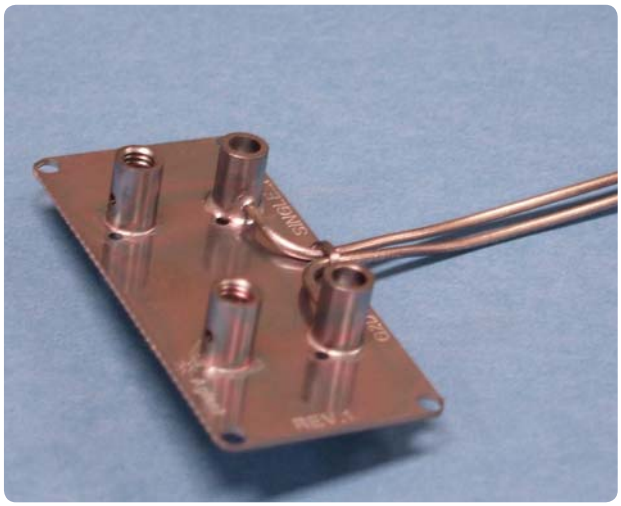


Figure 3. Agilent's modulator design includes specialized fittings attached by projection welding.

A planar structure incorporates flow tees and collector channels (Figure 3). All external connections are made through specialized fittings incorporated by projection welding onto the plate, providing near-zero unswept volumes and leak-tight seals. Agilent's design includes two major innovations: a diffusion-bonded manifold plate and a metal ferrule connector. The plates are the basis for low-mass, low-dead volume devices that enable diversion and splitting of gas flows to create a number of previously difficult capillary configurations.

Similar to integrated circuit manufacturing, the forming of this flow architecture uses photolithographic techniques to create the channels on one or both of two plates that are bonded together to form a metallic sandwich containing the desired internal flow channels. The ability to create these channels and provide external flow connections over very small distances within the GC oven dramatically reduces dead volume. What's more, the low thermal mass of the integrated plate provides for efficient heat transfer that might otherwise result in thermal lag and cold spots in the sample path. Figures 4 through 7 show examples of subassemblies, fittings and finished devices typical of capillary-flow technology. These structures are chemically deactivated to reduce interaction with active compounds.

Figure 4. Photolithographic milling ensures precise channel geometry and low dead volume in capillary-flow devices.

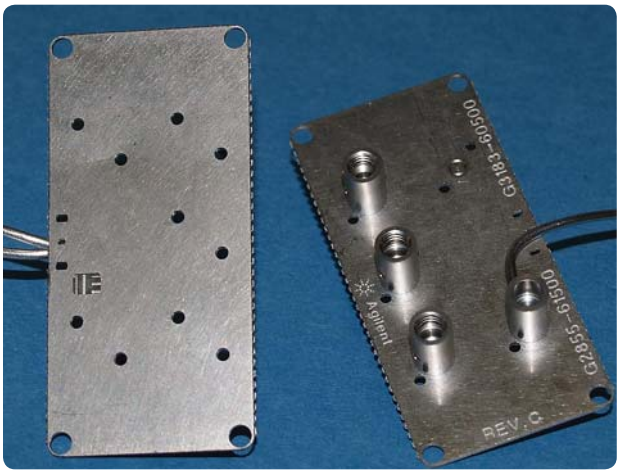


Figure 5. This photo shows top and inside views of a capillary-flow purged splitter.

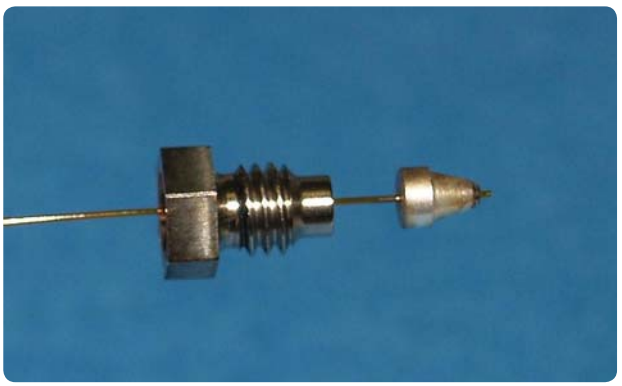


Figure 6. This subassembly provides a leak-tight connection to the modulator.

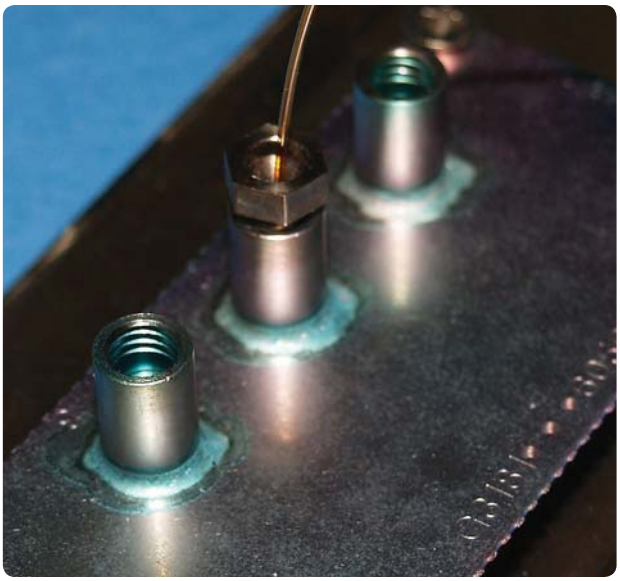


Figure 7. This close-up view shows a connection to a capillary flow device.

Outlining system functionality

Figures 8 and 9 illustrate the modulator. A three-way solenoid valve installed on top of the GC oven interfaces to a PCM module; the periodic switching of this solenoid drives the modulator. The precisely timed and synchronized switching between the "collect" and "flush" states directs discrete sample pulses continuously to the second column for additional fast separation during the entire chromatographic run.

Typical experimental parameters

GC:	Agilent 7890A
Detector:	FID at 200-Hz data collection rate, split/splitless inlet
Carrier:	Hydrogen
Column 1:	30 m x 0.25 mm x 0.25 um HP-5 ms, 19091S-433
Column 1:	Pressure: 21.5 psig at 50° C, constant flow mode
Column 2:	5 m x 0.25 mm x 0.15 um INNOWAX
Column 2:	Flow: 20 ml/min, constant flow mode
Oven program:	50° C (1.0 min) to 260° C (4 min) at 8° C/min.
Modulator period:	1.4 seconds collect, 0.12 second flush
2D analysis software:	GC Image (www.gcimage.com)

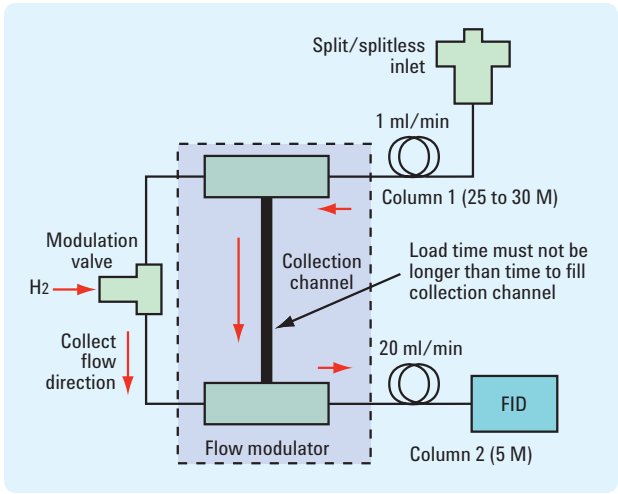


Figure 8. This diagram shows the flow rates and flow directions during the load or "collect" portion of the modulation cycle.

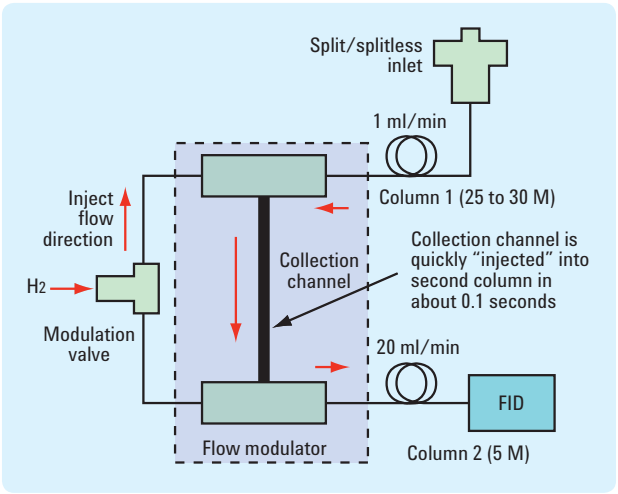


Figure 9. This diagram shows the flow rates and flow directions during the transfer or "inject" portion of the modulation cycle.

Load or collect state (Figure 8)**:** The primary column effluent containing analytes exits the first column after undergoing initial separation at the top tee. The second column flow, sourced by the PCM through the solenoid, enters at the bottom tee. In this configuration, first-column analytes will fill the collection channel; some compression occurs in the channel due to elevated pressure at the first-column exit.

Inject or flush state (Figure 9)**:** Flow from the solenoid is directed to the top tee. A high flow of typically 20 ml/min rapidly flushes the collection channel, transferring material in a very narrow band onto the second column where any analytes in the channel undergo rapid separation.

Capillary columns and speed: Total analysis time in a typical 2D GC system is essentially the same as with a 1D setup. A 2D chromatographic method will use oven temperature programs and column dimensions (25 to 30 m x 0.25 mm ID) similar to those in a 1D system. The typical goal is to achieve maximum peak capacity and display the maximum number of well-separated discrete compounds. Higher temperature program rates and shorter columns with smaller ID can be used; however, this may sacrifice separation for overall reduction of analysis time. A typical column set consists of a low-polarity column coupled to a very short (3 to 5 m) polar column (both with 0.25 mm ID). The second column must be very short to provide separation of all injected analytes during a typical 1.5-second modulation cycle or be driven at high-temperature program rates in a separate oven module.

Applying 2D GC

Figure 10 shows unmodulated and modulated peaks of a pure analyte (n-butylbenzene with approximately four modulations across the peak). Each modulated peak is very narrow due to the focusing effect of the modular and the speed of transfer to the second column. The peak height increases relative to the unmodulated peak since all mass is conserved. Ideally, the areas of the modulated peaks should equal the area of the unmodulated peak; the areas were within three percent for this test. Peak widths at half height for modulated butylbenzene are approximately 65 to 75 ms. Very narrow peaks are required for the technique to work properly and those shown in Figure 10 are similar to those obtained with thermal modulation systems.

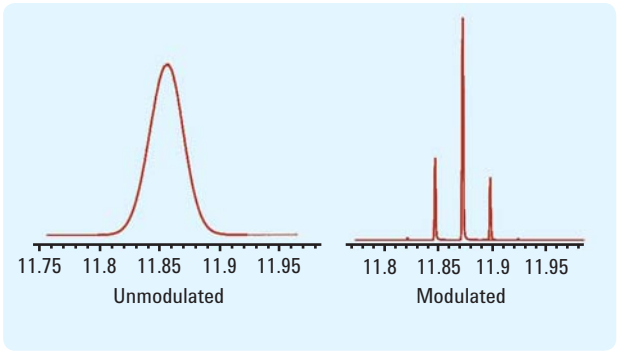
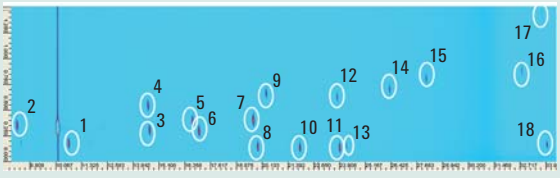


Figure 10. This comparison of unmodulated and modulated n-butylbenzene peaks from a hydrocarbon test sample provides a check of modulator performance and timing.

After checking for peak shapes and mass conservation, a performance test sample is run to verify the separation results and check for wrap-around effects (Figure 11). Wrap around is an undesirable consequence of compounds not completing elution from the second column during the modulation cycle in which they were injected.



1. Octane
2. Fluorobenzene
3. Propylbenzene
4. Bromo-2-fluorobenzene
5. Indane
6. Butylbenzene
7. Tetralin
8. Dodecane
9. Naphthalene
10. Tridecane
11. Tetradecane
12. Fluorobiphenyl
13. 1, 3, 5-Tributylbenzene
14. Acenaphthalene
15. Fluorene
16. Terphenyl
17. 2-Methylanthracene
18. Elcosan

Figure 11. This 2D GC display verifies the separation results from the hydrocarbon test sample.

The ability to visualize hydrocarbon class separations is a major attraction of 2D GC. Using non-polar column followed by a polar column produces hydrocarbon type retention in the following order: 1) alkanes, 2) cyclic alkanes, 3) olefins, 4) single-ring aromatics and 5) multi-ring aromatics. Figure 12 shows a 2D image of kerosene: Chemical classes are clearly discernible for all of these petrochemical materials, especially the aromatics.

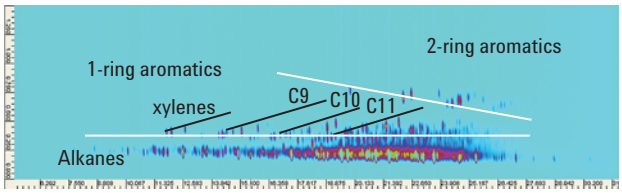


Figure 12. The one-ring and two-ring aromatics are clearly visible in this 2D measurement of kerosene.

Processing the acquired data

Specialized software is required to extract information from 2D GC data. Generally, the data are presented in a two-dimensional flat view where the retention time for the first dimension is along the "x" axis in minutes and the retention time of the second dimension is along the "y" axis in seconds. The software parses the chromatogram or raw data into this construct given knowledge of the modulation period (Figure 13). In visualization, the elution of chemical compounds from the two columns produces a cluster of pixels with values greater than background; colors are used to represent intensity or chemical amount. Figure 14 shows a 2D image based on the parsing of a raw modulated chromatogram.

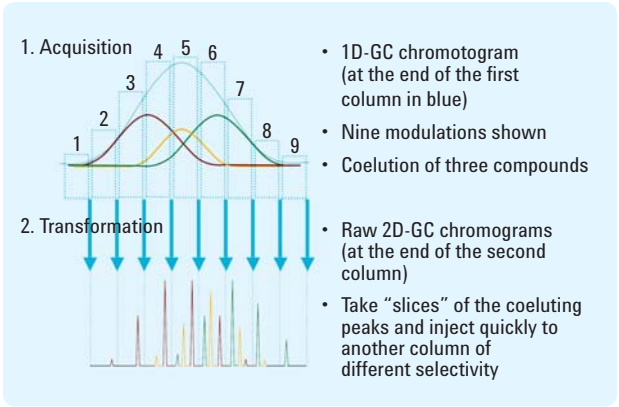


Figure 13. After GCxGC modulation, the red peak elutes last, the green peak elutes first and all three are completely separated.

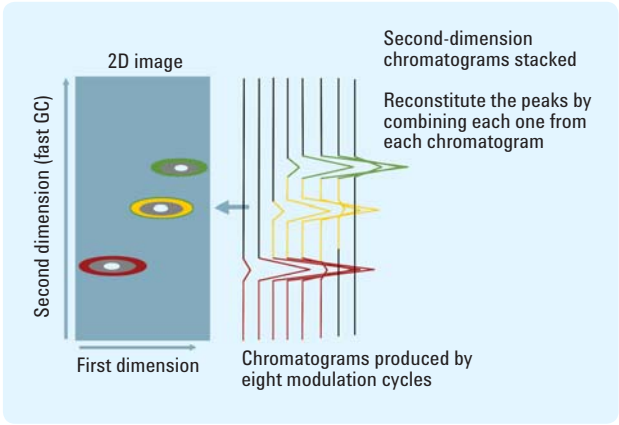


Figure 14. To visualize data in two dimensions, the modulated chromatograms are assembled as shown here.

These 2D images lend themselves to pattern recognition techniques. Principal component analysis (PCA), a data reduction tool used to classify samples, can be a powerful quality assurance (QA) tool when applied to final characterization of other complex products such as coffee, flavors and perfumes (Figure 15). This shows the potential to apply common chemometric pattern-recognition tools for sample classification to discern product differences, quality, adulteration and authenticity.

Note that the applications described in this article use a 1D flame ionization detector; however, the technique lends itself to coupling with a mass spectrometer to provide another dimension and confirmatory compound identification. Time-of-flight (TOF) mass spectrometers are typically used due to the need for high data collection rates. Quadrupole-based mass spectrometers such as the Agilent 5975C may also be used in limited-scan or selected ion monitoring (SIM) data acquisition modes of operation.

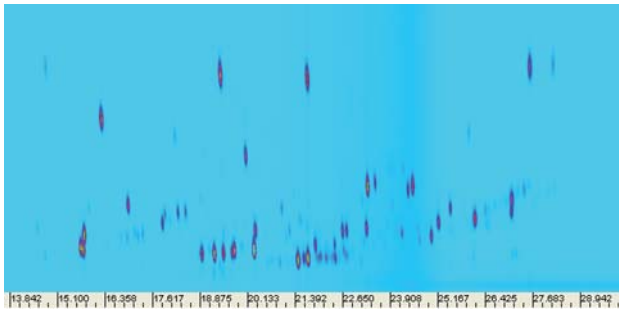
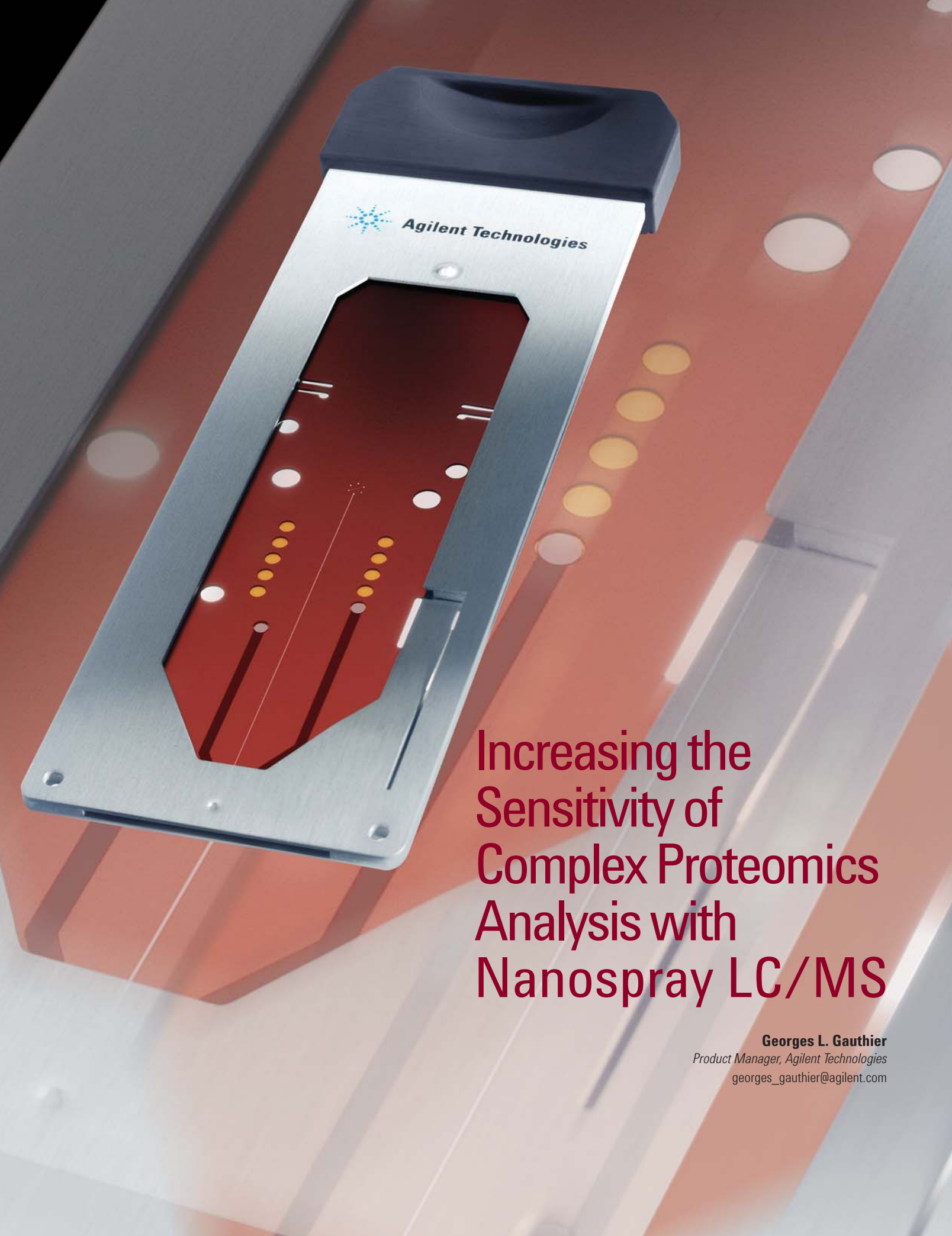


Figure 15. 2D GC can be used as a quality assurance tool for final characterization of complex products such as perfumes (shown).

Conclusion

For more than 10 years, 2D GC has been largely confined to the research laboratory, used only by skilled practitioners of gas chromatography. With reliable, easy-to-use hardware integrated into the gas chromatograph, the technique is now ready for more routine lab settings. Much of this is made possible by the advanced fabrication methods embodied in Agilent's capillary flow technology, and through firmware and software control of the resulting devices.

Extracting informative results depends on processing of 2D-GC data — and this remains a significant challenge. Specifically, quantitation requires more effort compared to traditional 1D GC and well-established hyphenated techniques such as GC/MS. In the next few years, however, we expect to see significant advances as 2D GC becomes better known and more widely used.



Increasing the Sensitivity of Complex Proteomics Analysis with Nanospray LC/MS

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Success in complex proteomics analysis often depends on the ability to work with very small or very dilute samples.

Techniques with names such as "nanoflow" and "nanospray" are being coupled with liquid chromatography/mass spectroscopy (LC/MS) to provide highly sensitive, highly specific analyses — even when working with just a few nanoliters of sample.

In these cases, nanoflow LC/MS has often been the method of choice despite the challenges associated with the use of small-inside-diameter capillaries and the need to keep such systems completely free of leaks, blockages and excessive dead volumes. A typical nano-LC setup is comprised of relatively complex plumbing that includes five key elements:

- An enrichment column to remove salts and concentrate the samples
- A separation column
- A microvalve to switch flows between the columns
- A nanoelectrospray emitter
- The capillaries and fittings that connect all components

To enhance this process, Agilent has integrated most of these components onto a single microfluidic device called a high-pressure liquid chromatography chip or HPLC-Chip. Smaller than a credit card, the reusable HPLC-Chip integrates enrichment column, separation column, hydraulic connections and nanospray emitter on a single biocompatible polymer chip.

Solvent and sample delivery to the chip, high-pressure switching of flows and automated chip loading and positioning in the MS source are accomplished with the companion HPLC-Chip Cube MS interface module. The HPLC-Chip Cube includes a microvalve for flow switching and everything else needed to couple the HPLC-Chip to the Agilent 1200 Series HPLC-Chip/MS system. This approach provides greater sensitivity, robustness, reliability and ease-of-use in nanoelectrospray MS applications such as proteomics, metabolomics and small-molecule separations.

Shrinking the components

Figure 1 shows the components and flows for a typical nanoflow LC/MS system. Such a system requires flow switching that enables loading of the sample (at high flow rates) onto the enrichment column, flushing onto the separation column and then analysis via nanoflow LC/MS/MS.

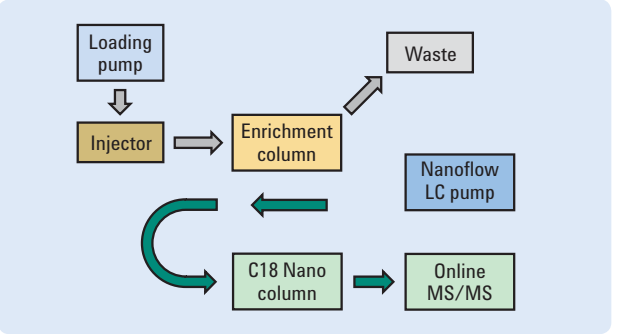

Figure 1. This diagram shows the flows through a conventional nanoflow LC/MS system with sample enrichment.

The HPLC-Chip, in combination with the HPLC-Chip/MS interface, replaces the columns, plumbing connections and flow-switching microvalve used in the nanoflow LC/MS setup. Figure 2 shows a schematic of the HPLC-Chip. The chip format is very flexible and allows for various combinations of sample cleanup and one- or two-dimensional nanoflow HPLC analyses.

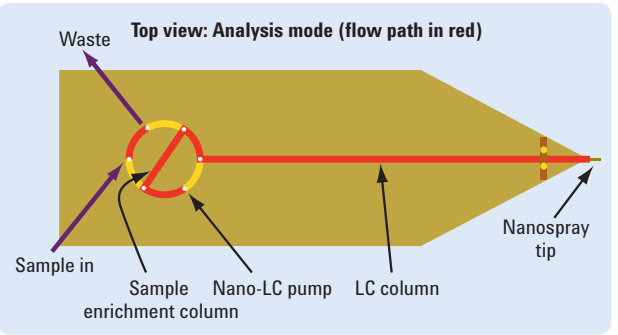

Figure 2. This schematic shows the inner workings of the HPLC-Chip.

The chip is fabricated from polyimide film, a material that is resistant to most solvents, tolerates a wide pH range, and is compatible with the analysis of proteins, peptides and a wide range of small molecules. The fabrication process uses ultraviolet (UV) laser ablation in combination with vacuum lamination of the polyimide film to create a multilayer microfluidic device.[1] Open micro-channels are packed with reversed-phase column materials to create HPLC columns. Metals are applied via thin-film deposition onto the polymer film surfaces to produce the electrical contacts for electrospray.

The finished chip also includes an embedded radio frequency (RF) tag that tracks usage and operating parameters. Information in the RF tag is automatically downloaded and updated by the system software.

Automating the connections

As shown in Figure 3, the HPLC-Chip is inserted into the HPLC-Chip Cube MS interface. The interface contains a loading mechanism for chip positioning, a microvalve for nano-LC hydraulic connections and flow switching and a nanospray ion source with camera for spray visualization. The HPLC-Chip Cube automatically — and precisely — positions the chip spray emitter orthogonally to the MS inlet, ensuring maximum sensitivity. It also makes the necessary electrical connections and all hydraulic connections to the chip. The entire process is fully automated and requires no tools.

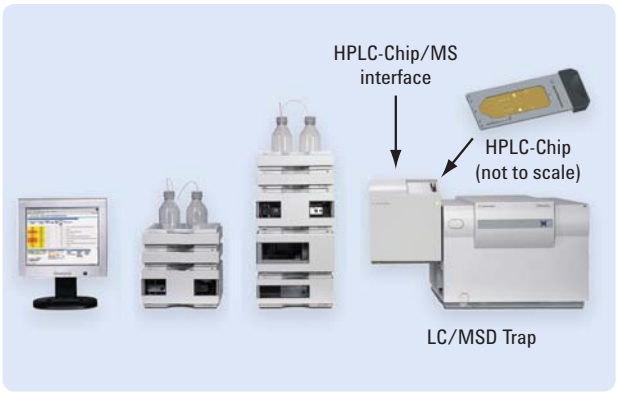

Figure 3. The HPLC-Chip is simply inserted into the HPLC-Chip Cube MS interface.

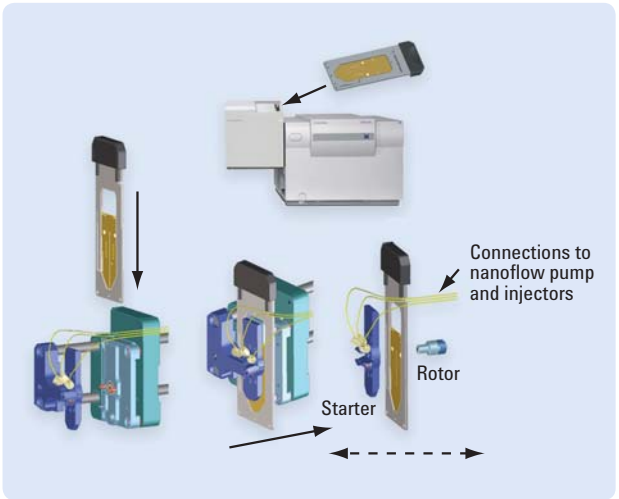

Figure 4. The interface automatically loads, connects and positions the chip.

With the Agilent 1200 Series nanoflow LC, micro well-plate autosampler and capillary sample loading pump directly connected to the HPLC-Chip Cube, the chip is automatically loaded, and leak-tight fluid connections are established by sandwiching the chip between the rotor and stator of the built-in multiport microvalve (Figure 4). The rotor and stator dock onto the chip and align the flow path from the nano-LC and loading pump to the port on the chip surface. Moving the rotor ensures quick and reliable switching between different flow paths such as sample enrichment and sample analysis.

The multiport microvalve utilizes a rotor-in-rotor design that uses a fixed stator with dual concentric rotors to deliver the solvents and sample to the different layers of the HPLC-Chip (Figure 5). Each rotor can operate independently and can rotate a full 360 degrees in one-degree steps. The number of possible connections is almost inexhaustible, ensuring compatibility with current HPLC-Chips as well as future designs that may incorporate features such as multidimensional columns and on-chip chemistries.

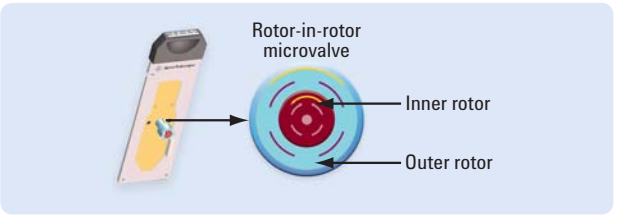

Figure 5. The inert multiport microvalve allows fluid delivery to even the most complex HPLC-Chip designs.

Comparing measurement results

The sensitivity of this technique is documented in several Agilent application notes, including *Comparison of HPLC-Chip MS with conventional nanoflow LC/MS for proteomic analyses.*[2] In that note, a direct comparison shows that the HPLC-Chip/MS system produces better chromatography and sensitivity in yeast proteome analysis, leading to more identified peptides and proteins.

All analyses were performed on the same instrument using either an orthogonal nanospray ion source or an HPLC-Chip/MS interface. All analyses used the same Agilent HPLC samplers and pumps and Agilent LC/MSD ion trap mass spectrometer. Data reduction was accomplished with the Agilent Spectrum Mill MS Proteomics Workbench software. Identical procedures and criteria were chosen in all experiments for MS and MS/MS data processing, protein database searches and results validation. Finally, every analysis was performed in triplicate.

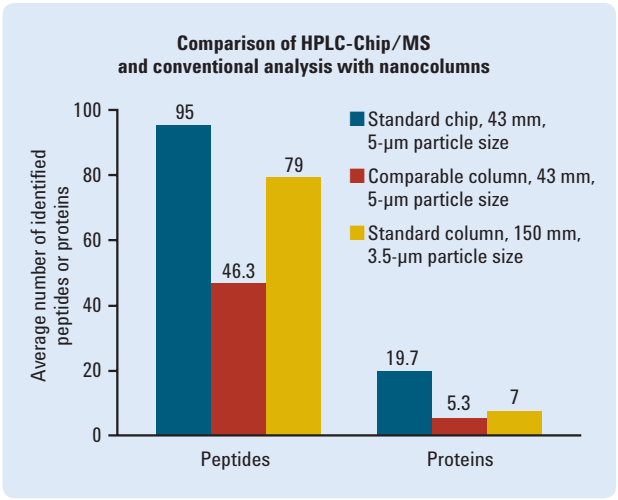

Figure 6. The HPLC-Chip identified more peptides and detected more proteins than the conventional method.

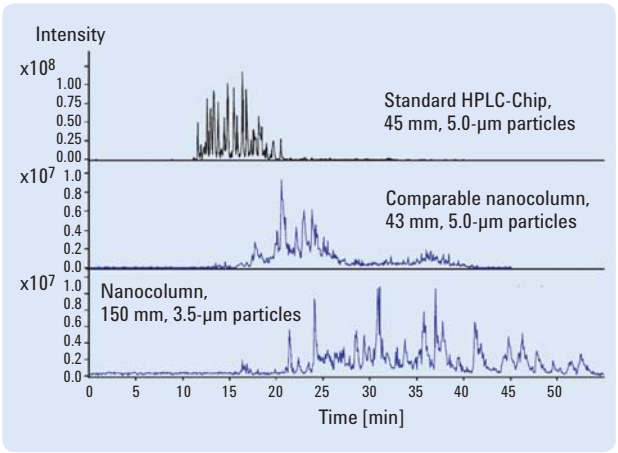

Figure 7. The HPLC-Chip provided better resolution and superior peak shape than conventional nanoflow.

Figure 6 presents the average numbers of identified peptides and proteins from the triplicate runs. These results clearly demonstrate that the number of identified peptides and the number of detected proteins were significantly greater with the HPLC-Chip/MS system than with the conventional nanoflow LC/MS system. This was the case not only when the HPLC-Chip and nanocolumn of similar dimensions were compared (43-mm length) but also when the chip was tested against a 150-mm nanocolumn.

The superior results of the HPLC-Chip are attributable to better chromatography and improved sensitivity. A comparison of base peak chromatograms taken under the three different conditions shows increased resolution and superior peak shape for the separation performed with the HPLC-Chip (Figure 7).

Understanding the improved analysis

A number of factors contributed to improved analysis with the HPLC-Chip/MS. First, component integration on the HPLC-Chip eliminated most of the plumbing connections, thereby reducing dead volumes. Second, sample adsorption was minimized using biocompatible polyimide and eliminating connectors susceptible to sample adsorption. Third, because the electrospray emitter is integrated into the HPLC-Chip, post-column peak dispersion was negligible. Overall, the optimized design of the sample pathway minimized sample loss and reduced dead volume.

An additional benefit was observed with the HPLC-Chip/MS: a high degree of reproducibility between repetitive analyses. Figure 8 illustrates this for the proteins identified from a database search of three sequential runs of the same sample. Fifteen out of 21 proteins were found in all of the analyses and only two proteins were identified from a single analysis.

Figure 8. The HPLC-Chip provided a high degree of reproducibility between repetitive analyses.

Conclusion

Complex proteomics analysis can benefit from the microfluidic approach embodied in the combination of the Agilent HPLC-Chip and HPLC-Chip Cube MS interface. Integrating sample enrichment, sample separation and a nanoelectrospray emitter on the HPLC-Chip enables better results, faster setup, superior repeatability and greater ease-of-use than traditional nanoflow LC/MS systems. In direct comparison to conventional nanoflow LC/MS — and using the same instrument — the HPLC-Chip/MS produced more protein identifications and provided a high degree of reproducibility from run to run.

References

1. Yin, H., Killeen, K., Brennen, R., Sobek, D., Werlich, M., and van de Goor, T., *Microfluidic Chip for Peptide Analysis with an Integrated HPCL Column, Sample Enrichment Column, and Nanoelectrospray Tip,* Analytical Chemistry, 77 (2), 2005, pp. 527-533.
2. Agilent publication number 5989-3538EN available from www.agilent.com.

Detecting Suspicious Intrusions into Next-Generation Networks

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Threats against corporate and personal data stored on computers are on the rise and an increasing amount of sensitive information is vulnerable to theft. As a result, more and more companies and individuals may suffer financial loss because of attacks on computer systems and networks.

Protecting this sensitive data requires a variety of approaches including anti-virus, anti-spyware, anti-phishing capabilities, firewalls and intrusion detection systems. Some of these provide remedial protection; others take a more active, preventive role. Intrusion detection is one of these and it relies on high-speed matching and recognition of patterns carried within network payloads.

In joint research supported by Agilent's University Grants Program, Agilent and the University of Kent investigated the effectiveness of a pattern-matching scheme that used a finite state machine (FSM) to implement a practical high-speed, low-cost, low-powered intrusion-detection probe. Such a scheme potentially addresses the key tradeoff between network speed and system flexibility while delivering a solution that offers a potentially small footprint and a reasonable cost.

The University of Kent designed a software system that takes a set of strings and produces a string-matching engine encoded in VHSIC Hardware Description Language (VHDL). This engine was tested using a VHDL simulation and a set of test data to represent network traffic.

Kent's engine was then modified by Agilent Laboratories to provide an infrastructure for its operation on a real Gigabit Ethernet network. The modifications also included the addition of mechanisms that reprogram the rules on-the-fly and report, on a per packet basis, the patterns observed within the network traffic.

The prototype was based on a Xilinx field-programmable gate array (FPGA) development board that supported Gigabit Ethernet. An FPGA is an ideal prototyping vehicle and it is easily able to consume traffic at full line rate. Tests were run on a private network using a subset of the Snort and Hogwash intrusion-detection rules. [1, 2]

Scoping the problem

The problem with traditional approaches to table-based FSM matching is that they do not scale well with word size because there will be 2^n possible input values for an n-bit data input. If an automaton is built as a simple lookup table then the amount of memory required very quickly becomes impractical; however, larger word sizes are key to monitoring high speed links, especially at Gigabit rates and higher.[3]

To circumvent this issue, a software pre-processor runs a number of algorithms that, for a given set of search strings, produces tables to compress the input data and a set of automata able to recognize those search strings in the compressed input data stream. The input to the automata is actually codified into a single numerical input that represents received bytes; this is called the symbol set and is derived from the union of all potential input patterns. Importantly, the numerical value used to represent the inputs can be easily extended to multi-byte input data (the value is unimportant so long as it is unambiguous and consistent).

Defining the symbol set

As an example, the search string "ABCDEF" and a four-byte input word produces the following symbol set:

Symbol set =
(***A, **AB, *ABC, ABCD, BCDE, CDEF, DEF*, EF**, F***, ****)

This represents all possible four-byte patterns on all byte alignments and includes matching of starting or ending patterns within an input word. The **** pattern indicates that none of the other patterns were found.

For input into the automaton we need only a four-bit bus to carry a numerical value that represents each pattern (e.g., "***A" = 0 ... up to ... "*****" = 9). Unfortunately, input data may match more than one symbol in the set and there is no way to prioritize the matching without loss. To circumvent this problem, two sets of input symbols are used:

Primary set = (ABCD, BCDE, CDEF, DEF*, EF**, F***, ****)
Secondary set = (*ABC , **AB, ***A, ****)

This avoids missing the start of new patterns when one ends and another begins within the same input data word. By allocating decreasing priority with the number of wildcards, the system will have exactly one match in each of the two symbol sets and therefore suffers no loss of input information. The system will now have two inputs to each FSM. A two-dimensional lookup table is used to create the combined outputs (Table 1).

Table 1. A two-dimensional lookup table creates the combined FSM inputs

	ABCD	BCDE	CDEF	DEF*	EF**	F***	****
***ABC**	◆	◆	◆	◆	◆	FABC	*ABC
****AB**	◆	◆	◆	◆	EFAB	F*AB	**AB
*****A**	◆	◆	◆	DEFA	EF*A	F**A	***A
*****	ABCD	BCDE	CDEF	DEF*	EF*	F***	****

The merged symbol set is as follows:

(ABCD, BCDE, CDEF, DEFA, DEF*, EFAB, EF*A, EF**, FABC, F*AB, F**A, F***, *ABC, **AB, ***A, ****)

The table operates on the numerical values representing each pattern; the actual values are not important but must be consistent. This operation is referred to as the merge stage. The ◆ entries in the table are impossible and are left undefined. Figure 1 shows the resulting single-pattern matching unit.

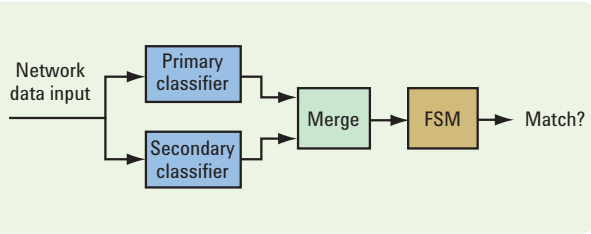


Figure 1. A single-pattern matching unit

Enabling multiple-pattern matching

A complete system is actually more complex than this. First, an efficient way to compress the input data is needed. For word sizes greater than eight bits this must be done in stages because of the potential size of the compression tables required. The first step is to compress each eight bits of the input individually and then use one or more combine stages, each of which merges together two input busses — and this further compresses the output at the same time.

The compressed input data then passes through one or more group stages, each of which takes a single input bus and compresses it in different ways on its output ports. The outputs from the final group stage provide the inputs to the pattern-matching automata. A simple compression system for a 16-bit input with a single-level group stage is shown in Figure 2.

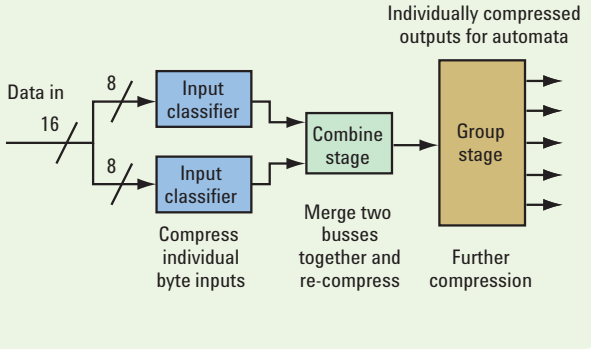


Figure 2. Example input-compression system, with a 16-bit data input

Using sparse arrays and Aho-Corasick matching

Unfortunately, the multiple-pattern matching approach still produces a very large set of sparsely populated tables. As a consequence, we investigated a data compression system for sparse arrays for both the combine stage and the automata tables. The algorithm called row displacement with state marking is used in compilers and has been implemented for these components within an FPGA by Sugawara, et al.[4, 5] By using this technique in conjunction with Aho-Corasick's multi-string matching automata, we observed a significant reduction in table size.[6, 7] This requires a more complex design for the merge stage, which now uses a lookup table to deal with many combinations of starts and ends of different strings that might occur in an input data word for multi-string automata.

The final architecture is able to operate with only a single level group stage, as these now provide outputs that relate to the symbols for many different patterns. The combine stage and the automata tables both use sparse arrays to improve memory utilization.

Creating the code generator

The physical manifestation of the above architecture as a set of VHDL entities can vary depending on word size, clock rates, number of rules, dictionary size, number of patterns per automaton, target hardware and memory. A "one size fits all" implementation might not be appropriate for a particular application or target device. What's more, creating a VHDL description of the final hardware is challenging because complex algorithms are needed to generate the look-up tables, create the automata, populate the various stages and construct the required busses.

To cope with this complexity, pre-processing is performed by a Java-based program running on a PC with the RAM tables created as appropriately sized arrays in memory. Each VHDL entity — bus, RAM, FSM, hardware clock, input classifier and the various stages — has a corresponding Java implementation and a simulation can be run by driving data, byte by byte, through the software instantiation of the system.

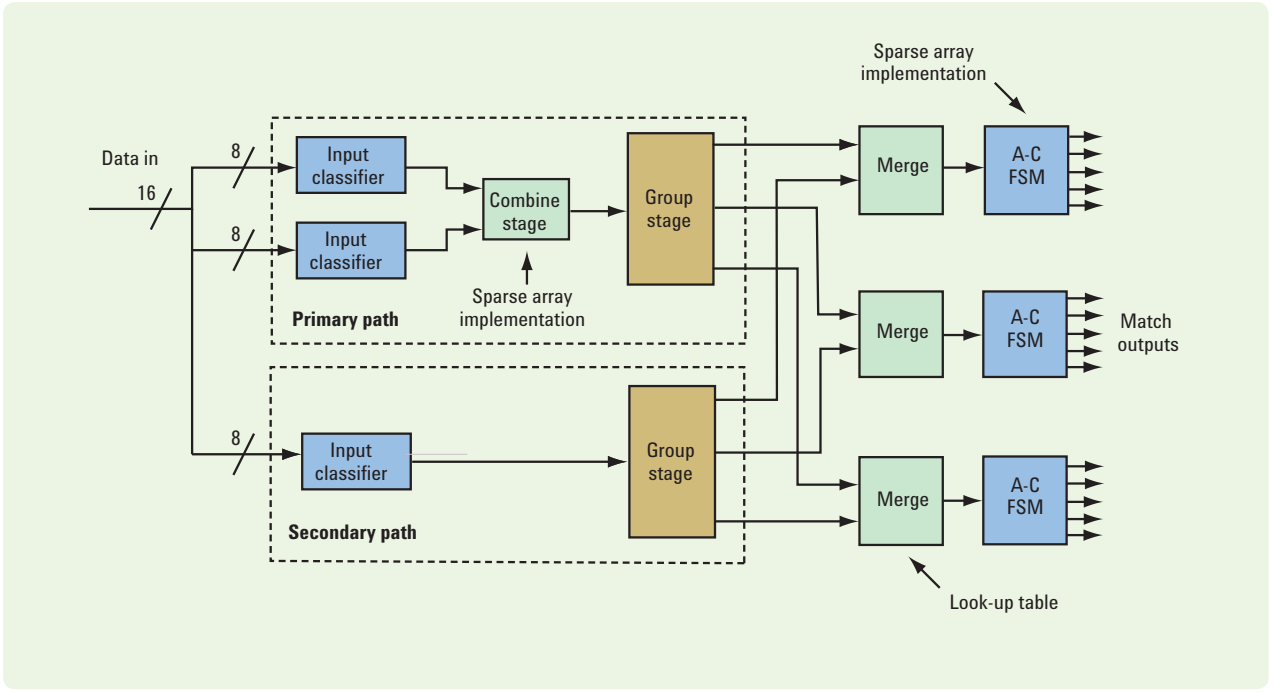


Figure 3. The final architecture

Early versions of the software allowed us to vary many of the pre-processor's input parameters. However, the end goal is a working prototype so VHDL or similar is required. Again, creating the VHDL is non-trivial and, to reduce the complexity, we fixed several parameters (e.g., defining a 16-bit bus width). We also selected the number of strings per automaton to make best use of the FPGA's Block RAM units. The RAM tables were created as INIT statements embedded in VHDL. These were compiled with ModelSim and bench tested against a set of test data using the same input rules.

Implementing on the lab bench

Having a test bench that consumes "canned" test data is a far cry from a working prototype able to recognize suspicious events on a live network. The network's data must be decoded into the 16-bit input bus of the matching engine. Gigabit Ethernet transmits bytes serially that are eight-bit, 125-MHz GMII encoded with an 8B/10B scheme developed from Fiber Channel, taking the fiber bit rate of 1000 Mb/s to 1.25 Gbaud. The encoding provides for DC balance, run-length limiting, and simple de-serializer alignment; idle code sets are used to aid clock recovery even when no data is being transferred.

The probe was implemented on a Virtex II Pro XC2VP20 FPGA, which has much of the required input/output infrastructure built into its Rocket IO units. By parsing only the data frames and ignoring idle and preamble codes, the probe can extract just the packet payload and pass this to the matching engine (only the payload is of interest because headers cannot carry harmful strings). Of course, the engine never stops processing, and because it consumes data during every clock cycle, we set a "don't care" bit on the input and a match is never produced by data that is not payload. The created FPGA image is downloaded using an on-board diagnostic connection and the prototype is ready to match network traffic.[8]

Processing a match

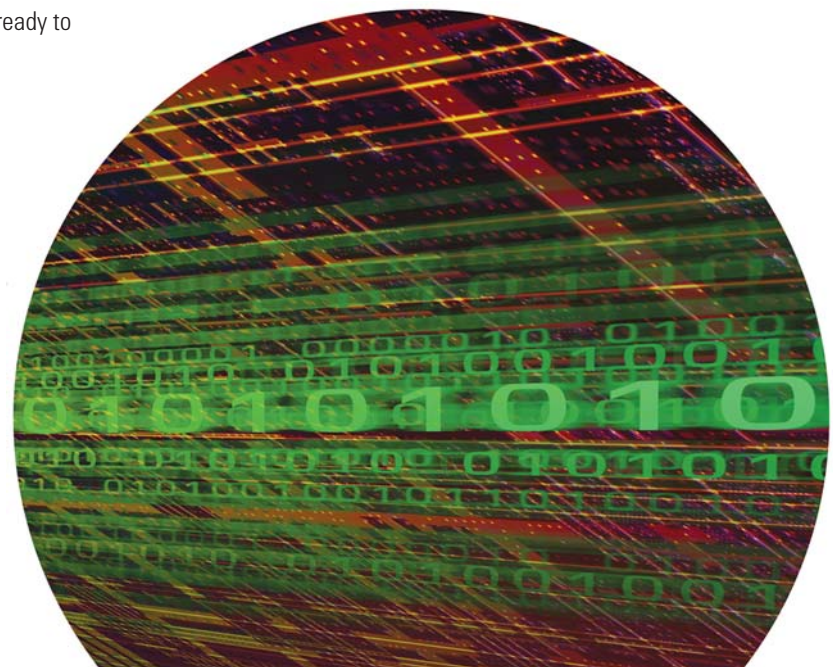
When a match occurs, one or more rules could be matched one or more times within a packet. If a rule is matched at least once within a packet's payload, the probe reports a match as a bit vector that has each bit corresponding to a matched rule set to "true." A latch is used so that subsequent matches within the same payload cause the bit to remain set. All latches are cleared at the end of the packet and actions can be taken depending upon which rules were matched.

Changing the rules

When the monitoring device is installed on a network at key gateways, it will need periodic updates with new rules that detect new threats. Memory is finite, and so once the device is full, the system operator will also have to expire the old rules in favor of newer threats.

Getting the new rules into an operating detector is a critical problem. Programming through a diagnostic port is not practical, so we devised a process in which the new tables are generated offline by the pre-processor. The high level of compression involved and the lack memory on the FGPA precludes incremental changes so completely new tables are required each time the rules are altered. The new tables are then encapsulated into a series of sequenced packets and sent to the device.

We tested this on the development board by sending packets over a Gigabit link. When the FPGA receives the first packet it enters configuration mode and stops matching. New tables are loaded as they arrive and once the last table is loaded, the engine starts to scan using the new rules.



Summarizing the results

As used on the development board, the Virtex II Pro FPGA has 88 Block RAM units, each of 18 Kb in size.[9] The firmware is configured to use 16 Kb; for ease of implementation the parity bits are not used and the system is able to store approximately five to eight rules per 16 Kb of RAM, depending upon rule length. However, a certain fixed overhead for both the packet decoding infrastructure and matching engine is required. For a rule set based upon 76 of the Hogwash rules, the design uses 38 Block RAM units.[2] Approximately 28 of the RAM units are fixed overhead with four of these being used for non-application-related infrastructure, netting 0.45 RAM units per rule. This leaves space for somewhere between 240 and 384 rules, and only 20 percent of the available logic is used.

Larger chips in the same family, for example the XC2VP40, support 192 RAM units, so more rules could be accommodated. Reconfiguration of the rules requires 68 packets, each containing half a RAM unit (about 35 KB of data). The time spent offline for reconfiguration is much less than one second but depends on network delays. At this rule capacity, the design has a maximum clock speed of well over 130 MHz, which is twice the requirement so the device is therefore capable of monitoring two input channels or one bidirectional link. Maximum rule length has been tested at 128 bytes, although in theory higher lengths are possible, limited only by the size of a single memory unit on the target device.

Conclusion

This method has performed well when tested at Gigabit link rates and has demonstrated that by employing appropriate compression techniques a viable number of rules can be stored in an FPGA. The baseline version utilized 1.7 RAM units per rule whereas the last tested version uses 0.45 RAM units per rule and has a storage ratio that, as a result of the compression process, actually improves with larger rule sets. As a consequence, Agilent has a awarded a second grant to the University of Kent to continue their work in this field. Among other things, the new project will look into further increasing rule density and support for much higher data rates including up to 10 Gigabits per second. A number of interesting challenges lie ahead.

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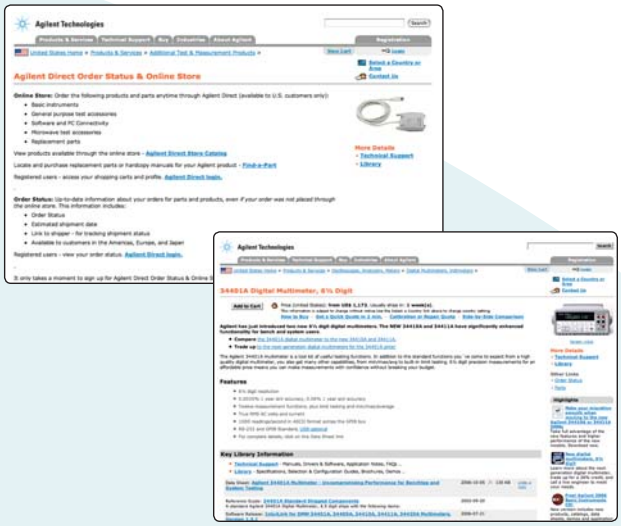

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